

Model Name: P35-S3

Rev2.01

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	POWER MAP
05	P4 LGA775 A
06	P4 LGA775 B
07	P4 LGA775 C
08	P4 LGA775 D
09	GMCH-BEARLAKE HOST
10	GMCH-BEARLAKE DDRII
11	GMCH-BEARLAKE PCI E, DMI
12	GMCH-BEARLAKE INT VGA
13	GMCH-BEARLAKE GND
14	GMCH-BEARLAKE PWR
15	DDRII CHANNEL A 1,2
16	DDRII CHANNEL B 1,2
17	DDRII TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH9 PCI, USB, DMI, LAN
20	ICH9 GPIO, CTRL
21	ICH9 SATA, FAN PWM
22	ICH9 VCC, GND
23	CLOCK GEN CK505
24	PCI EXPRESS*1 ,PCI SLOT 1,2
25	ITE8718/GB,RESET DRIVE
26	COM,LPT
27	BIOS,CI,HWM,KB/MS

SHEET

TITLE

28	AZALIA ALC889A
29	AUDIO JACK
30	VCORE PWM ISL6327
31	DISCRETE POWER
32	ATX POWER
33	JMicron JMB363
34	LAN REALTEK RTL8111B
35	FRONT PANEL,FUSB,FDD

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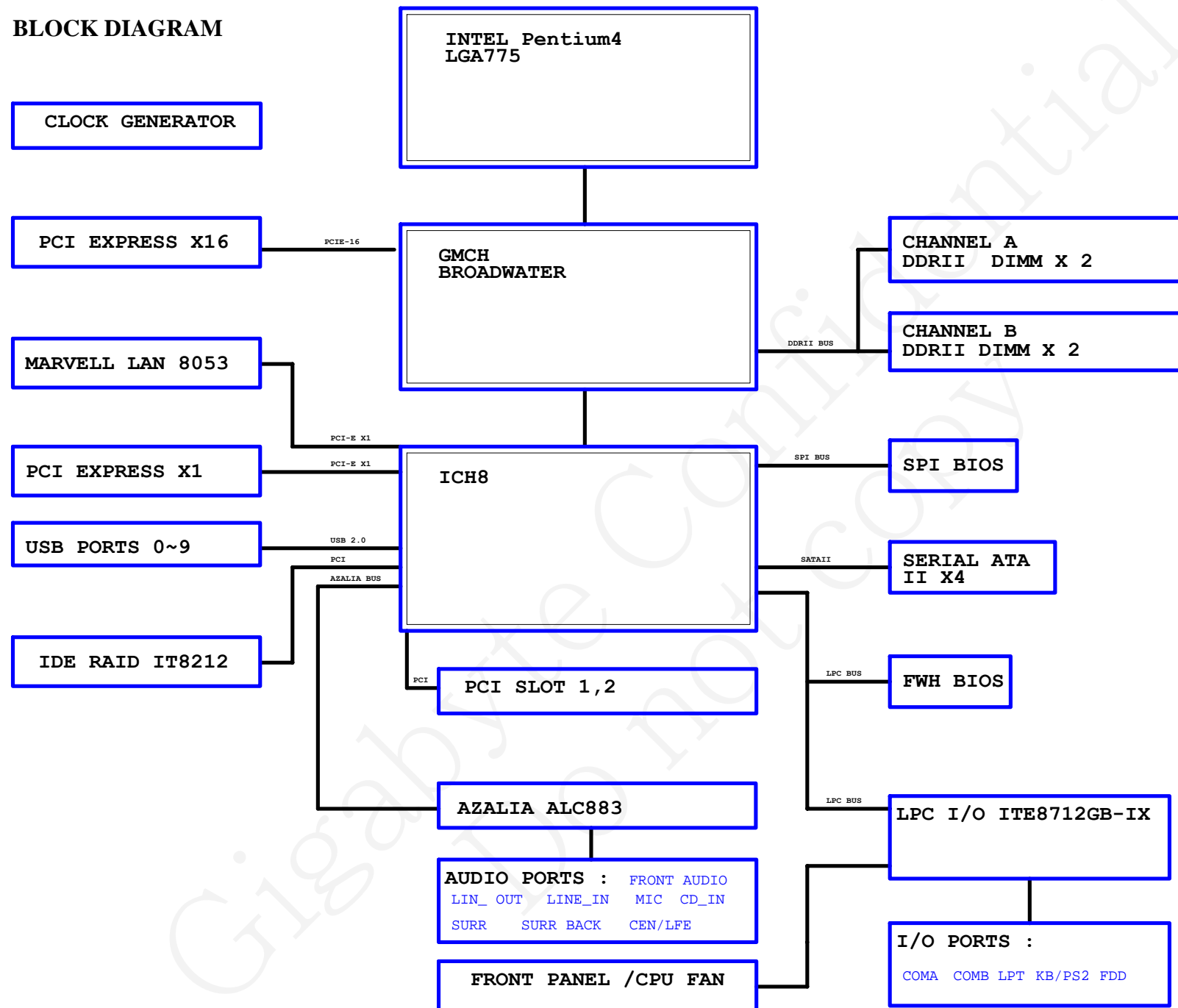
Cover Sheet			
Size	Document Number	P35-S3	Rev
Custom			2.01
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Circuit or PCB layout change  
for next version

Component value change history

Data	Change Item	Reason
0.1A	EVT release	
0.2A	1. VTT_GMCH Q329 AP40T03 --> 2SK9918	
	2. VCORE CHOKE 0.5uH Footprint Change & 料號修改	
	3. IOUT DR100 100K --> 20K	
	4. PCB 智恩 REMOVE	
	5. PWM5,PWM6 阻值修改	
	6. CHOKE FOOTPRINT MODIFY	
	7. ADD COAXIAL:11NR6-501004-83R	
	8. REMOVE VGA , CHANGE TO COM	
	9. REMOVE HDMI_AC	
	10. PWM MOSFET MODIFY	
0.2B	1. BC115,BC729 2.2u/6/Y5V/10V/Z --> 2.2u/6/Y5V/6.3V/Z	
	2. ADD 8P4R(0402) 8.2K : 10RN3-048201-16R	
	3. ITE8718 REV.EX --> GX	
	4. U55只保留RT9199,其餘移除	
	5. VCC1_25 CAP 560uF --> 820uF	
1.0A	1. U55 ADD 替料 10GL2-206137-01R	
	2. UPDATE GMCH/A2 料號	
	3. ISL6545 OCP CHANGE R2007,R2009 15K/4 --> 8.2K/4	
	4. AP40T03H --> NEC3918	
	5. ALC889 PIN40 CR2 20K/4/1 --> 20K/4/0.1	
	6. VCORE MOSFET ADD VENDOR:INFINEO	
	7. RCA REMOVE 11NR6-501004-83R	
	8. 5VDUAL PROTECT R2057 390K/4 --> 150K/4	
1.0B	1. 增加包材	
	2. N/B CHANGE 新料號	
	3. MODIFY VCORE LOAD LINE RISISTOR	
	4. Q36 替料移除10GL6-501084-07R/09R	
	5. DU2,U50,U52 替料移除10TA1-200324-05R	
	6 -RSMRST C1329 0.1u/6 --> 0.01u/6	
	7. -PWRBTSW ADD 限流電阻 R2077=33/4	

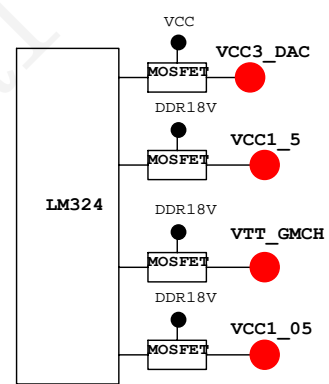
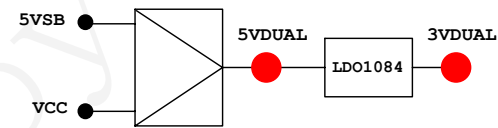
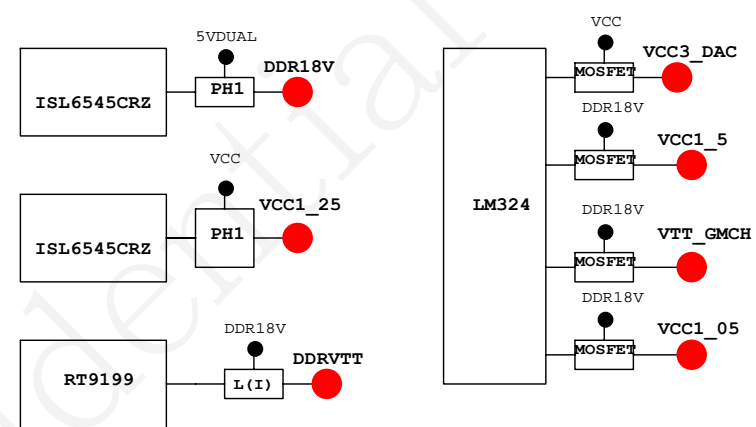
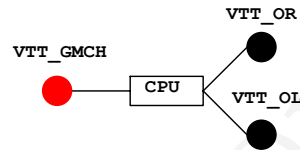
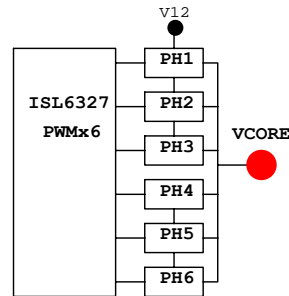
DATE	Change Item	Reason
0.1	EVT release	
0.2	1. CHOKE 0.5uH 1.2uH 2uH Footprint Change	
	2. BSEL166_4 GP46 --> GP41	
	3. DDR18V_OV1~OV3 ITE8718 --> ICH9 GPIO	
	4. ADD CPU GTLREF_UV0~UV1 GPIO CONTROL	
1.0	1. Remove All 0 ohm	
	2. OS-CON CAP 底下的零件要移除 (AUDIO)	
	3. DL15 FOOTPRINT CHANGE "CHOKE08U-15A_1P-2"	
	4. LGA775 FOOTPRINT CHANGE "LGA775-39"	
	5. SB_HEATSINI --> SB_HEATSINK	
	6. BEARLAKE機種PCB要導入文字面	
	7. 5VDUAL PROTECT ADD D18	
1.01	1.北橋 HEATSINK 擋住 MODEL 文字面	
	2. DL9~DL14 "CHOKE05U-30A-1PQ-1" --> "CHOKE05U-30A-1PQ-2"	
	3. -PWRBTSW ADD 限流電阻 R2077=33/4	
1.02	1. 移除"Ultra Durable 2"	
	2. ADD NB_HEATSINK 外框	
	3. 文字面修改 DDRII 800/1066 (OC)--> DDRII 800/1066	
2.8	1. JMB363 CHANGE TO E-SATA	
	2. F_USB2,3 --> R_USB2,3	
	3. ADD OP+MOSFET補償線路	
	4. R.G.B & HDMI REMOVE	
	5. LPT CHANGE TO CONNECT 2*13K24	
	6. CHECNGE CONNECT FOR SPDIF I & SPDIF_O	
	7. RTL8111B & RTL8111C CO-LAYOUT	
2.81	1. JMB363 E-SATA --> ICH9R PORT4_5 E-SATA	2. RCA_SPDIF FOOTPRINT UPDATE
BOM		3. NB_HEATSINK 改 4上2下
P35-DS3R-10C	1. CPU GTLREF0~3 RATIO 0.67 --> 0.63 2. REMOVE VIN CAP DBC3 1u/8	4. OP+MOSFET 補償線路修改
10D	1. EC176 560uF --> 820uF For VCC1_05 Shake	2.0
10E	1. REMOVE R2038 8.2K/4	1. JMB363 & ICH9R還原成REV1.02 2. 後圖改8個USB
1.02		3. RTL8111C CO-LAYOUT UPDATE
10G 10H	1. PCB REV1.01 --> REV1.02 1. C1388 1u/6/Y5V/10V/Z --> 1u/6/X5R/10V/K (STR Fail on high temp.)	2.01 螺絲孔修改
2.8 28A	1. PCB REV1.02 --> REV2.8	
28B	1. N/B HEATSINK 改成 12SP2-040007-2*R 2. REMOVE R2078,R2079,R2080 20K/4/1 3. REMOVE C1427,C1428,C1429 1N/4/X7R/50V/K	
28C	1. PCB REV2.8 --> REV2.81	
20B-PVT	1. PCB REV2.0 --> 2.01 (螺絲孔修改) 2. 包材CHECK	

**BLOCK DIAGRAM**

ICH8 GPIO LIST TABLE

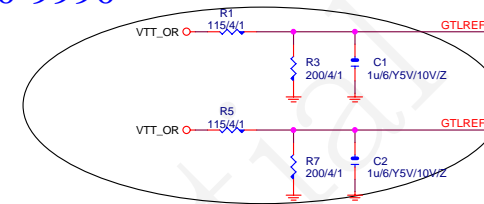
PIN NAME	PWR WELL	AFTER/ PLTRST	USAGE	NOTE
GP0	MAIN	IN	-ACZ_DET	P/U 8.2K VCC3
GP1/TACH1	MAIN	IN	ICH_FAN_TACH1	P/U 8.2K VCC3
GP2/PIRQE#	MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	IN	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	IN	ICH_FAN_TACH2	P/U 8.2K VCC3
GP7/TACH3	MAIN	IN	ICH_FAN_TACH3	P/U 8.2K VCC3
GP8	STBY	IN	GPIO8 (DUALBIOS_INPUT)	P/U 8.2K 3VDUAL
GP9	STBY	OUT	WOL_ONLY	P/D 100K GND
GP10	STBY	IN	CLGPIO1	P/U 8.2K 3VDUAL
GP11/SMBALERT#	STBY	OUT	-SMBALRT	P/U 8.2K 3VDUAL
GP12	STBY	IN	MB_ID0	P/U 8.2K 3VDUAL
GP13	STBY	IN	-LPCPME	P/U 8.2K 3VDUAL
GP14	STBY	IN	CLGPIO2	P/U 8.2K 3VDUAL
GP15	STBY	OUT	LAN_DISABLE (STP_PCI-)	N/A
GP16	MAIN	OUT/LOW	RESET	N/A
GP17/TACH0	MAIN	IN	ICH_FAN_TACH0	P/U 8.2K VCC3
GP18	MAIN	OUT	MB_ID1	P/U 8.2K VCC3
GP19	MAIN	IN	SATA1GP	P/U 8.2K VCC3
GP20	MAIN	OUT	-SPI_WP0	P/U 1K 3VCL
GP21	MAIN	IN	SATA0GP	P/U 8.2K VCC3
GP22	MAIN	IN	SCLOCK	P/U 8.2K VCC3
GP23	MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	OUT	CLGPIO0	P/U 8.2K 3VDUAL
GP25	STBY	IN	MB_ID2 (STP_CPU-)	P/U 8.2K 3VDUAL
GP26/S4_STATE#	STBY	OUT	S4_STATE#	P/U 8.2K 3VDUAL
GP27	STBY	OUT/LOW	GPIO27 (EL_STATE0)	P/U 8.2K 3VDUAL
GP28	STBY	OUT/LOW	PWR_LED (EL_STATE1)	N/A
GP29/OC5#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP30/OC6#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP31/OC7#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP32	MAIN	OUT	DUAL_BIOS	P/U 100K+1M VCC3
GP33	MAIN	OUT	DUAL_BIOS	P/U 8.2K VCC3
GP34	MAIN	OUT/LOW	GPIO34/SMB_RST	N/A
GP35	MAIN	OUT	SATACLKREQ#	N/A
GP36	MAIN	IN	SATA2GP	P/U 8.2K VCC3
GP37	MAIN	IN	SATA3GP	P/U 8.2K VCC3
GP38	MAIN	IN	SLOAD	P/U 8.2K VCC3
GP39	MAIN	IN	GPIO39	P/D 8.2K GND
GP48	MAIN	IN	GPIO48	P/U 8.2K VCC3
GP49	MAIN	IN	CPUPWROK	P/U 100 VTT_OL

VCORE:6 PHASE PWM--ISL6327CRZ



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Title			
TABLE LIST			
Size B	Document Number		Rev
	P35-S3		2.0
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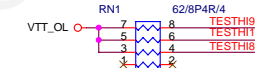
HA/REQ:4/11 50+-15%  
ADSTB:4/14 50+-15%



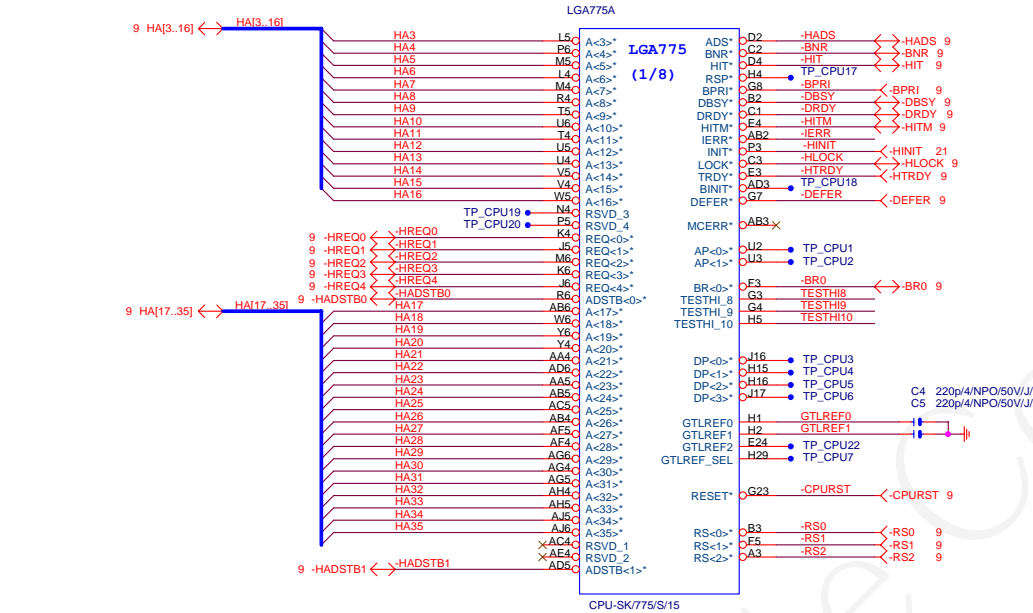
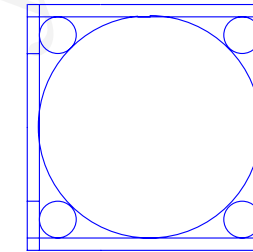
VTT\_OR R8 62/4 -IERR

VTT\_OL R10 62/4 -BR0

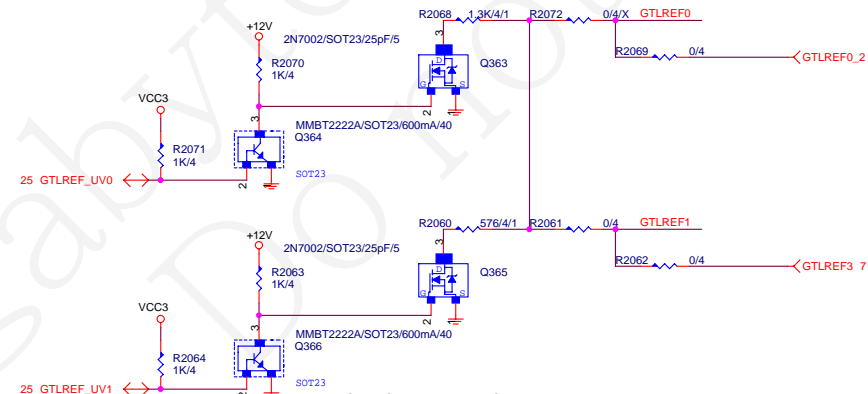
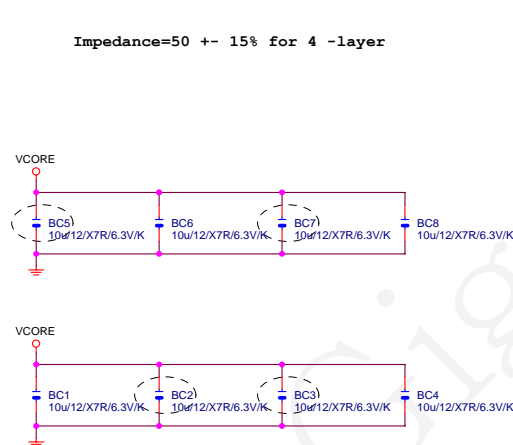
VTT\_OR R12 62/4 -CPURST



CR  
CPU RETENTION/X



Impedance=50 +- 15% for 4-layer

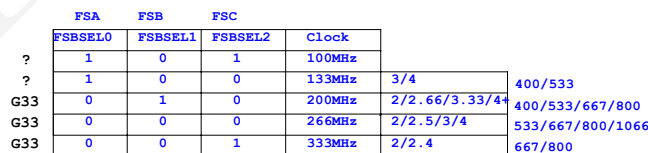


CPU GTLREF RATIO

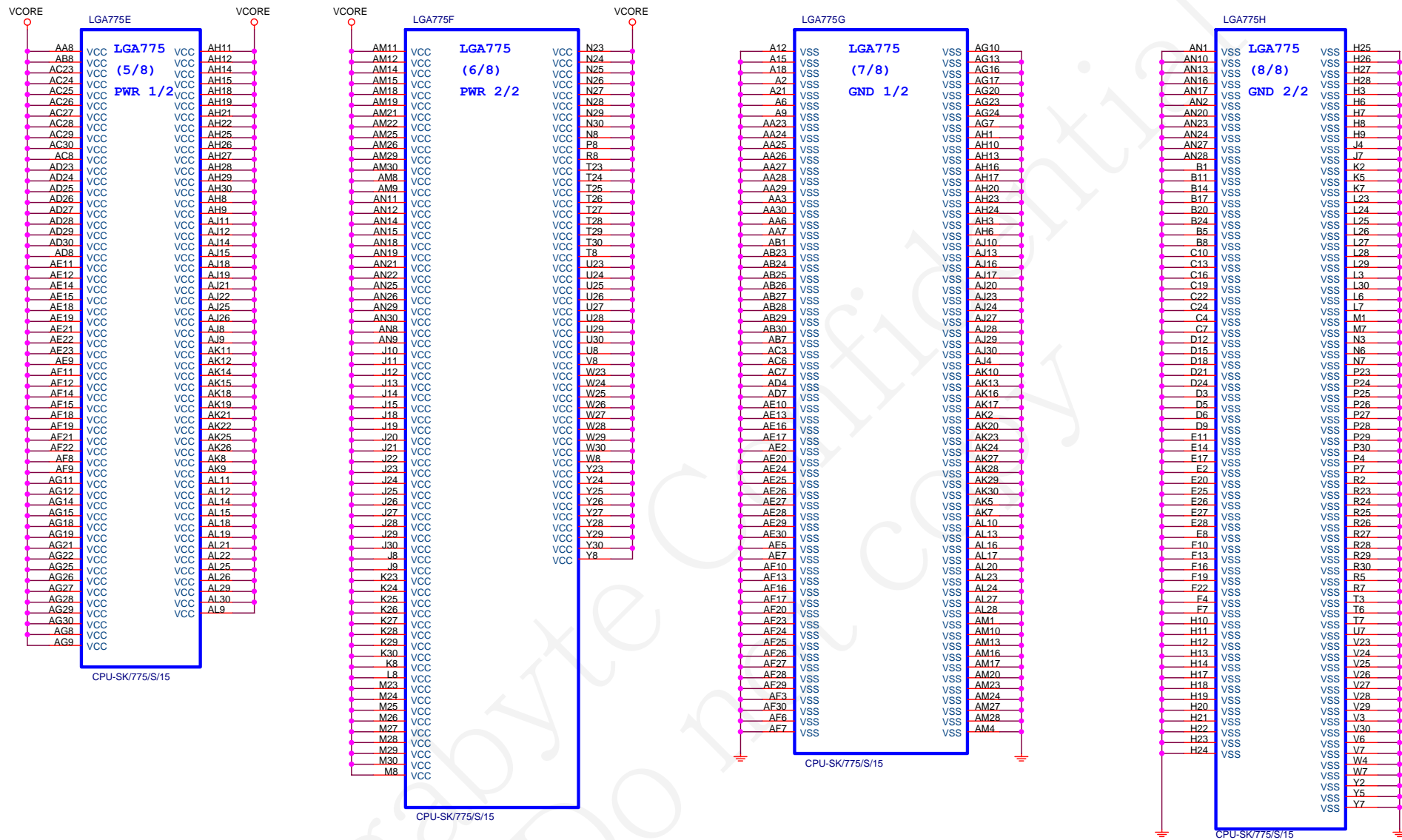
GTLREF_UV0	GTLREF_UV1	Ratio Set
HIGH	HIGH	0.67
LOW	HIGH	0.65
HIGH	LOW	0.63
LOW	LOW	0.615

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Title		
P4_LGA775-A		
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Custom	P35-S3	2.01
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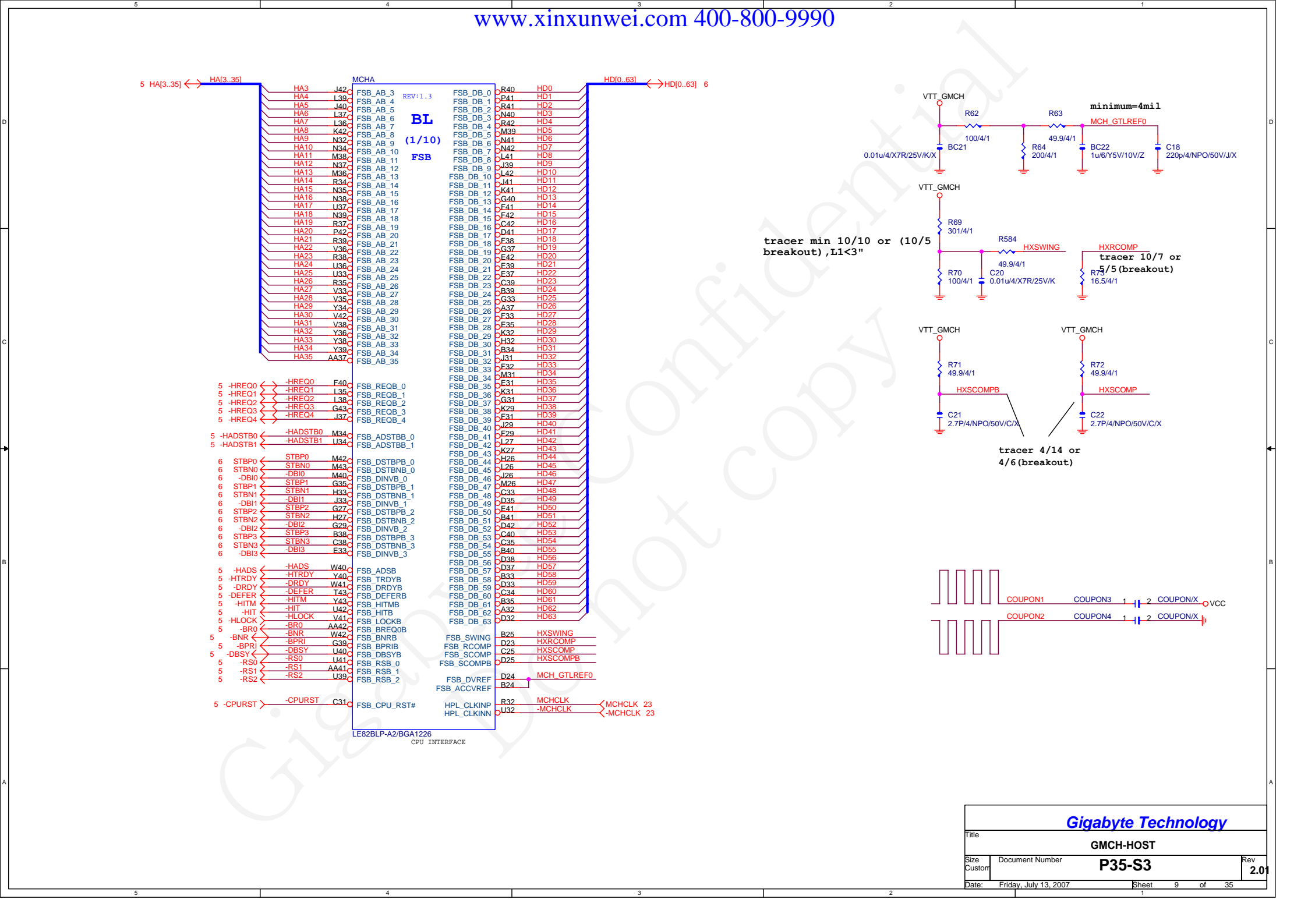
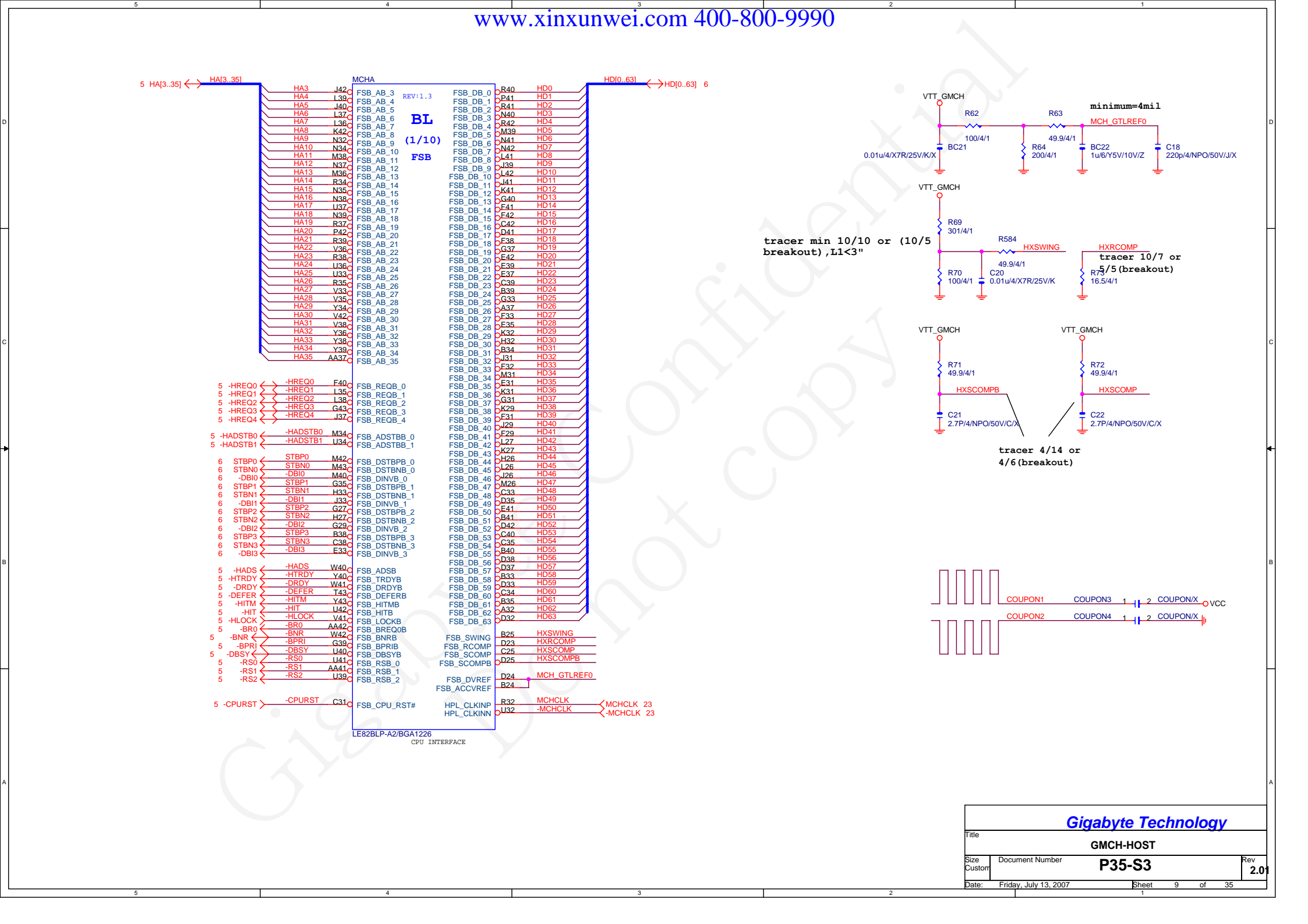
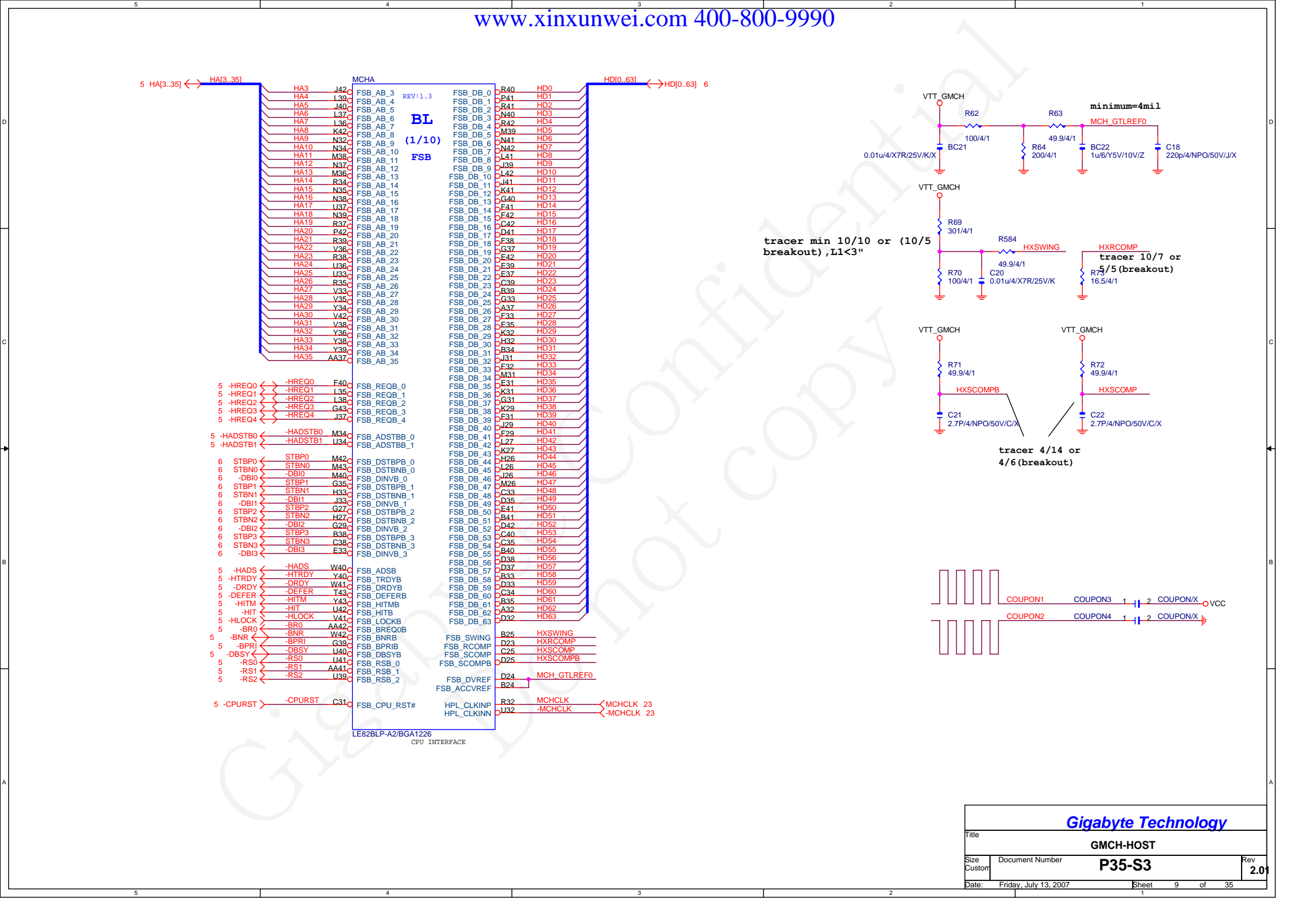




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Title			P4_LGA775-E,F,G,H	
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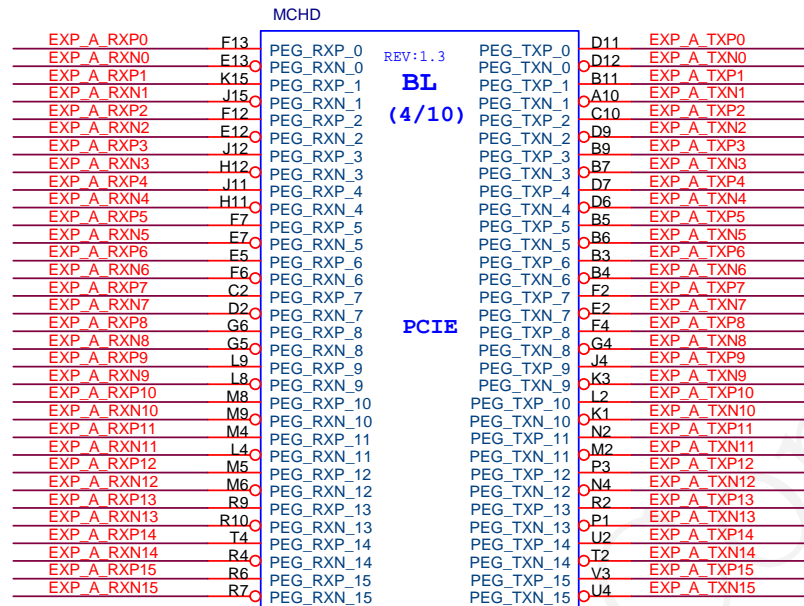


## MCHB

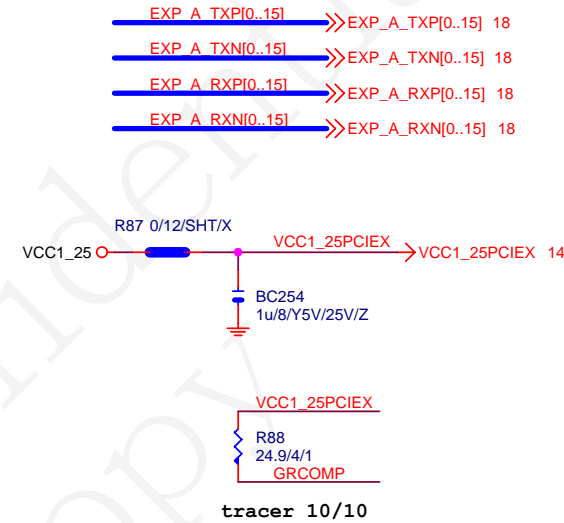
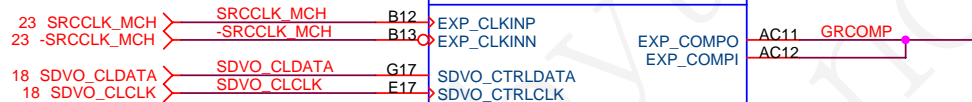
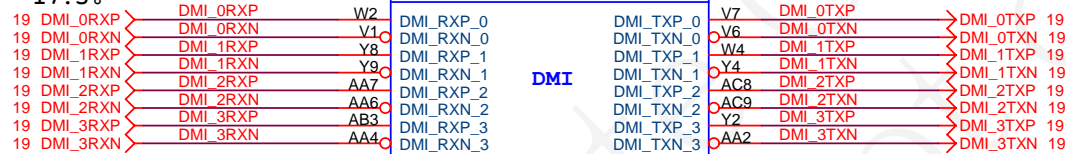
REV:1.3  
BL  
(2/10)  
DDR\_A

MAAA0	B630	DDR_A_MA_0	DDR_A_DQS_0
MAAA1	AY25	DDR_A_MA_1	DDR_A_DQS_1
MAAA2	BA23	DDR_A_MA_2	DDR_A_DM_0
MAAA3	B623	DDR_A_MA_3	
MAAA4	AY23	DDR_A_MA_4	
MAAA5	B622	DDR_A_MA_5	
MAAA6	BA22	DDR_A_MA_6	
MAAA7	B621	DDR_A_MA_7	
MAAA8	AY21	DDR_A_MA_8	
MAAA9	BA21	DDR_A_MA_9	
MAAA10	B611	DDR_A_MA_10	
MAAA11	AY21	DDR_A_MA_11	
MAAA12	BA20	DDR_A_MA_12	
MAAA13	AY38	DDR_A_MA_13	
MAAA14	BA19	DDR_A_MA_14	
15.17 -SWEA	-SWEA	DDR_A_WEB	DDR_A_DQS_1
15.17 -SCASA	-SCASA	DDR_A_CASB	DDR_A_DM_1
15.17 -SRASA	-SRASA	DDR_A_RASB	
15.17 SBA00	SBA00	DDR_A_BS_0	
15.17 SBA01	SBA01	DDR_A_BS_1	
15.17 SBA02	SBA02	DDR_A_BS_2	
15.17 CSA00	CSA00	DDR_A_CSB_0	
15.17 CSA01	CSA01	DDR_A_CSB_1	
15.17 CSA02	CSA02	DDR_A_CSB_2	
15.17 CSA03	CSA03	DDR_A_CSB_3	
15.17 CKEA0	CKEA0	DDR_A_CKE_0	
15.17 CKEA1	CKEA1	DDR_A_CKE_1	
15.17 CKEA2	CKEA2	DDR_A_CKE_2	
15.17 CKEA3	CKEA3	DDR_A_CKE_3	
MODT_A0	B635	DDR_A_ODT_0	
MODT_A1	BA38	DDR_A_ODT_1	
MODT_A2	BA35	DDR_A_ODT_2	
MODT_A3	BA39	DDR_A_ODT_3	
15 DCLKA0	DCLKA0	DDR_A_CK_0	
15 DCLKA1	DCLKA1	DDR_A_CK_1	
15 DCLKA2	DCLKA2	DDR_A_CK_2	
15 DCLKA3	DCLKA3	DDR_A_CK_3	
15 DCLKA4	DCLKA4	DDR_A_CK_4	
15 DCLKA5	DCLKA5	DDR_A_CK_5	
15 DCLKA6	DCLKA6	DDR_A_CK_6	
15 DCLKA7	DCLKA7	DDR_A_CK_7	
15 DCLKA8	DCLKA8	DDR_A_CK_8	
15 DCLKA9	DCLKA9	DDR_A_CK_9	
15 DCLKA10	DCLKA10	DDR_A_CK_10	
15 DCLKA11	DCLKA11	DDR_A_CK_11	
15 DCLKA12	DCLKA12	DDR_A_CK_12	
15 DCLKA13	DCLKA13	DDR_A_CK_13	
15 DCLKA14	DCLKA14	DDR_A_CK_14	
15 DCLKA15	DCLKA15	DDR_A_CK_15	
15 DCLKA16	DCLKA16	DDR_A_CK_16	
15 DCLKA17	DCLKA17	DDR_A_CK_17	
15 DCLKA18	DCLKA18	DDR_A_CK_18	
15 DCLKA19	DCLKA19	DDR_A_CK_19	
15 DCLKA20	DCLKA20	DDR_A_CK_20	
15 DCLKA21	DCLKA21	DDR_A_CK_21	
15 DCLKA22	DCLKA22	DDR_A_CK_22	
15 DCLKA23	DCLKA23	DDR_A_CK_23	
15 DCLKA24	DCLKA24	DDR_A_CK_24	
15 DCLKA25	DCLKA25	DDR_A_CK_25	
15 DCLKA26	DCLKA26	DDR_A_CK_26	
15 DCLKA27	DCLKA27	DDR_A_CK_27	
15 DCLKA28	DCLKA28	DDR_A_CK_28	
15 DCLKA29	DCLKA29	DDR_A_CK_29	
15 DCLKA30	DCLKA30	DDR_A_CK_30	
15 DCLKA31	DCLKA31	DDR_A_CK_31	
15 DCLKA32	DCLKA32	DDR_A_CK_32	
15 DCLKA33	DCLKA33	DDR_A_CK_33	
15 DCLKA34	DCLKA34	DDR_A_CK_34	
15 DCLKA35	DCLKA35	DDR_A_CK_35	
15 DCLKA36	DCLKA36	DDR_A_CK_36	
15 DCLKA37	DCLKA37	DDR_A_CK_37	
15 DCLKA38	DCLKA38	DDR_A_CK_38	
15 DCLKA39	DCLKA39	DDR_A_CK_39	
15 DCLKA40	DCLKA40	DDR_A_CK_40	
15 DCLKA41	DCLKA41	DDR_A_CK_41	
15 DCLKA42	DCLKA42	DDR_A_CK_42	
15 DCLKA43	DCLKA43	DDR_A_CK_43	
15 DCLKA44	DCLKA44	DDR_A_CK_44	
15 DCLKA45	DCLKA45	DDR_A_CK_45	
15 DCLKA46	DCLKA46	DDR_A_CK_46	
15 DCLKA47	DCLKA47	DDR_A_CK_47	
15 DCLKA48	DCLKA48	DDR_A_CK_48	
15 DCLKA49	DCLKA49	DDR_A_CK_49	
15 DCLKA50	DCLKA50	DDR_A_CK_50	
15 DCLKA51	DCLKA51	DDR_A_CK_51	
15 DCLKA52	DCLKA52	DDR_A_CK_52	
15 DCLKA53	DCLKA53	DDR_A_CK_53	
15 DCLKA54	DCLKA54	DDR_A_CK_54	
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15 DCLKA58	DCLKA58	DDR_A_CK_58	
15 DCLKA59	DCLKA59	DDR_A_CK_59	
15 DCLKA60	DCLKA60	DDR_A_CK_60	
15 DCLKA61	DCLKA61	DDR_A_CK_61	
15 DCLKA62	DCLKA62	DDR_A_CK_62	
15 DCLKA63	DCLKA63	DDR_A_CK_63	
15 DCLKA64	DCLKA64	DDR_A_CK_64	
15 DCLKA65	DCLKA65	DDR_A_CK_65	
15 DCLKA66	DCLKA66	DDR_A_CK_66	
15 DCLKA67	DCLKA67	DDR_A_CK_67	
15 DCLKA68	DCLKA68	DDR_A_CK_68	
15 DCLKA69	DCLKA69	DDR_A_CK_69	
15 DCLKA70	DCLKA70	DDR_A_CK_70	
15 DCLKA71	DCLKA71	DDR_A_CK_71	
15 DCLKA72	DCLKA72	DDR_A_CK_72	
15 DCLKA73	DCLKA73	DDR_A_CK_73	
15 DCLKA74	DCLKA74	DDR_A_CK_74	
15 DCLKA75	DCLKA75	DDR_A_CK_75	
15 DCLKA76	DCLKA76	DDR_A_CK_76	
15 DCLKA77	DCLKA77	DDR_A_CK_77	
15 DCLKA78	DCLKA78	DDR_A_CK_78	
15 DCLKA79	DCLKA79	DDR_A_CK_79	
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15 DCLKA83	DCLKA83	DDR_A_CK_83	
15 DCLKA84	DCLKA84	DDR_A_CK_84	
15 DCLKA85	DCLKA85	DDR_A_CK_85	
15 DCLKA86	DCLKA86	DDR_A_CK_86	
15 DCLKA87	DCLKA87	DDR_A_CK_87	
15 DCLKA88	DCLKA88	DDR_A_CK_88	
15 DCLKA89	DCLKA89	DDR_A_CK_89	
15 DCLKA90	DCLKA90	DDR_A_CK_90	
15 DCLKA91	DCLKA91	DDR_A_CK_91	
15 DCLKA92	DCLKA92	DDR_A_CK_92	
15 DCLKA93	DCLKA93	DDR_A_CK_93	
15 DCLKA94	DCLKA94	DDR_A_CK_94	
15 DCLKA95	DCLKA95	DDR_A_CK_95	
15 DCLKA96	DCLKA96	DDR_A_CK_96	
15 DCLKA97	DCLKA97	DDR_A_CK_97	
15 DCLKA98	DCLKA98	DDR_A_CK_98	
15 DCLKA99	DCLKA99	DDR_A_CK_99	
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15 DCLKA102	DCLKA102	DDR_A_CK_102	
15 DCLKA103	DCLKA103	DDR_A_CK_103	
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15 DCLKA105	DCLKA105	DDR_A_CK_105	
15 DCLKA106	DCLKA106	DDR_A_CK_106	
15 DCLKA107	DCLKA107	DDR_A_CK_107	
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PCIEX16:15/4/8/4/15  
Impedance=95 +- 17.5%

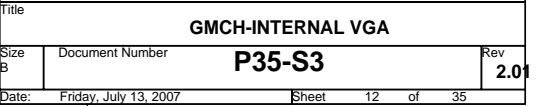


DMI:12/4/8/4/12  
Impedance=95 +- 17.5%



**Gigabyte Technology**

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GMCH-PCI E & DMI			
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MCHG

REV:1.3

BC37	VSS_1	VSS_181	AE24
BC32	VSS_2	VSS_182	AE22
BC28	VSS_3	VSS_183	AE20
BC24	VSS_4	VSS_184	AE4
BC10	VSS_5	VSS_185	AE3
BC5	VSS_6	VSS_186	AE2
BB7	VSS_7	VSS_187	AD42
AY41	VSS_8	VSS_188	AD39
AY4	VSS_9	VSS_189	AD37
AW43	VSS_10	VSS_190	AD35
AW41	VSS_11	VSS_191	AD33
AV37	VSS_12	VSS_192	AD25
AV35	VSS_13	VSS_193	AD23
AV27	VSS_14	VSS_194	AD21
AV23	VSS_15	VSS_195	AD19
AV21	VSS_16	VSS_196	AC38
AV17	VSS_17	VSS_197	AC35
AV11	VSS_18	VSS_198	AC24
AV9	VSS_19	VSS_199	AC22
AV7	VSS_20	VSS_200	AC20
AV2	VSS_21	VSS_201	AC10
AU42	VSS_22	VSS_202	AC7
AU38	VSS_23	VSS_203	AC5
AU32	VSS_24	VSS_204	AB43
AU24	VSS_25	VSS_205	AB25
AU20	VSS_26	VSS_206	AB23
AU16	VSS_27	VSS_207	AB21
AU4	VSS_28	VSS_208	AB19
AT31	VSS_29	VSS_209	AB2
AT29	VSS_30	VSS_210	AB1
AT15	VSS_31	VSS_211	AA38
AT13	VSS_32	VSS_212	AA35
AT12	VSS_33	VSS_213	AA24
AR38	VSS_34	VSS_214	AA22
AR33	VSS_35	VSS_215	AA20
AR32	VSS_36	VSS_216	AA8
AR27	VSS_37	VSS_217	AA5
AR26	VSS_38	VSS_218	Y42
AR23	VSS_39	VSS_219	Y37
AR21	VSS_40	VSS_220	Y35
AR20	VSS_41	VSS_221	Y33
AR17	VSS_42	VSS_222	Y25
AR9	VSS_43	VSS_223	Y23
AR6	VSS_44	VSS_224	Y21
AP43	VSS_45	VSS_225	Y19
AP24	VSS_46	VSS_226	Y10
AP18	VSS_47	VSS_227	Y7
AP1	VSS_48	VSS_228	Y5
AN38	VSS_49	VSS_229	Y1
AN31	VSS_50	VSS_230	W24
AN29	VSS_51	VSS_231	W22
AN24	VSS_52	VSS_232	W20
AN23	VSS_53	VSS_233	W3
AN20	VSS_54	VSS_234	V43
AN13	VSS_55	VSS_235	V39
AN12	VSS_56	VSS_236	V37
AN11	VSS_57	VSS_237	V34
AN4	VSS_58	VSS_238	V32
AM42	VSS_59	VSS_239	V11
AM40	VSS_60	VSS_240	V8
AM36	VSS_61	VSS_241	V5
AM33	VSS_62	VSS_242	V2
AM29	VSS_63	VSS_243	U38
AM24	VSS_64	VSS_244	U35
AM23	VSS_65	VSS_245	U8
AM20	VSS_66	VSS_246	U7
AM11	VSS_67	VSS_247	U5
AM9	VSS_68	VSS_248	T42
AM7	VSS_69	VSS_249	T1
AM4	VSS_70	VSS_250	R36
AL36	VSS_71	VSS_251	R33
AL33	VSS_72	VSS_252	R31
AL31	VSS_73	VSS_253	R11
AK43	VSS_74	VSS_254	R8
AJ39	VSS_75	VSS_255	R5
AJ36	VSS_76	VSS_256	R3
AJ33	VSS_77	VSS_257	P43
AJ32	VSS_78	VSS_258	P30
AH42	VSS_79	VSS_259	P21
AG37	VSS_80	VSS_260	P18
AG34	VSS_81	VSS_261	P17
AF43	VSS_82	VSS_262	P2
AF37	VSS_83	VSS_263	N36
AF36	VSS_84	VSS_264	N33
AF10	VSS_85	VSS_265	N31
AF9	VSS_86	VSS_266	N27
AF8	VSS_87	VSS_267	N21
AF7	VSS_88	VSS_268	N13
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LE82BLP-A2/BGA1226

MCHG

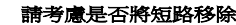
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M27	VSS_95	VSS_275	A18
M21	VSS_96	VSS_276	A12
M20	VSS_97	VSS_277	A7
M17	VSS_98	VSS_278	BC41
M15	VSS_99	VSS_279	BC3
M10	VSS_100	VSS_280	BA1
M7	VSS_101	VSS_281	AY40
M1	VSS_102	VSS_282	AF23
L40	VSS_103	VSS_283	AF21
L33	VSS_104	VSS_284	AF19
L32	VSS_105	VSS_285	AE18
L31	VSS_106	VSS_286	AC18
L29	VSS_107	VSS_287	AA18
L21	VSS_108	VSS_288	V29
L20	VSS_109	VSS_289	U27
L11	VSS_110	VSS_290	R21
L7	VSS_111	VSS_291	E1
L5	VSS_112	VSS_292	C43
L3	VSS_113	VSS_293	C1
K43	VSS_114	VSS_294	A41
K26	VSS_115	VSS_295	A5
K21	VSS_116	VSS_296	A3
K18	VSS_117	VSS_297	V30
K13	VSS_118	VSS_298	
K12	VSS_119		
K2	VSS_120		
J38	VSS_121		
J35	VSS_122		
J32	VSS_123		
J27	VSS_124		
J21	VSS_125		
J9	VSS_126		
J7	VSS_127		
J5	VSS_128		
H31	VSS_129		
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H13	VSS_135		
G42	VSS_136		
G38	VSS_137		
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F21	VSS_149		
F18	VSS_150		
F15	VSS_151		
F3	VSS_152		
E43	VSS_153		
E32	VSS_154		
E24	VSS_155		
E21	VSS_156		
E11	VSS_157		
E9	VSS_158		
E3	VSS_159		
D40	VSS_160		
D31	VSS_161		
D21	VSS_162		
D17	VSS_163		
D15	VSS_164		
D3	VSS_165		
C26	VSS_166		
C11	VSS_167		
C6	VSS_168		
C5	VSS_169		
C4	VSS_170		
B37	VSS_171		
B32	VSS_172		
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B26	VSS_174		
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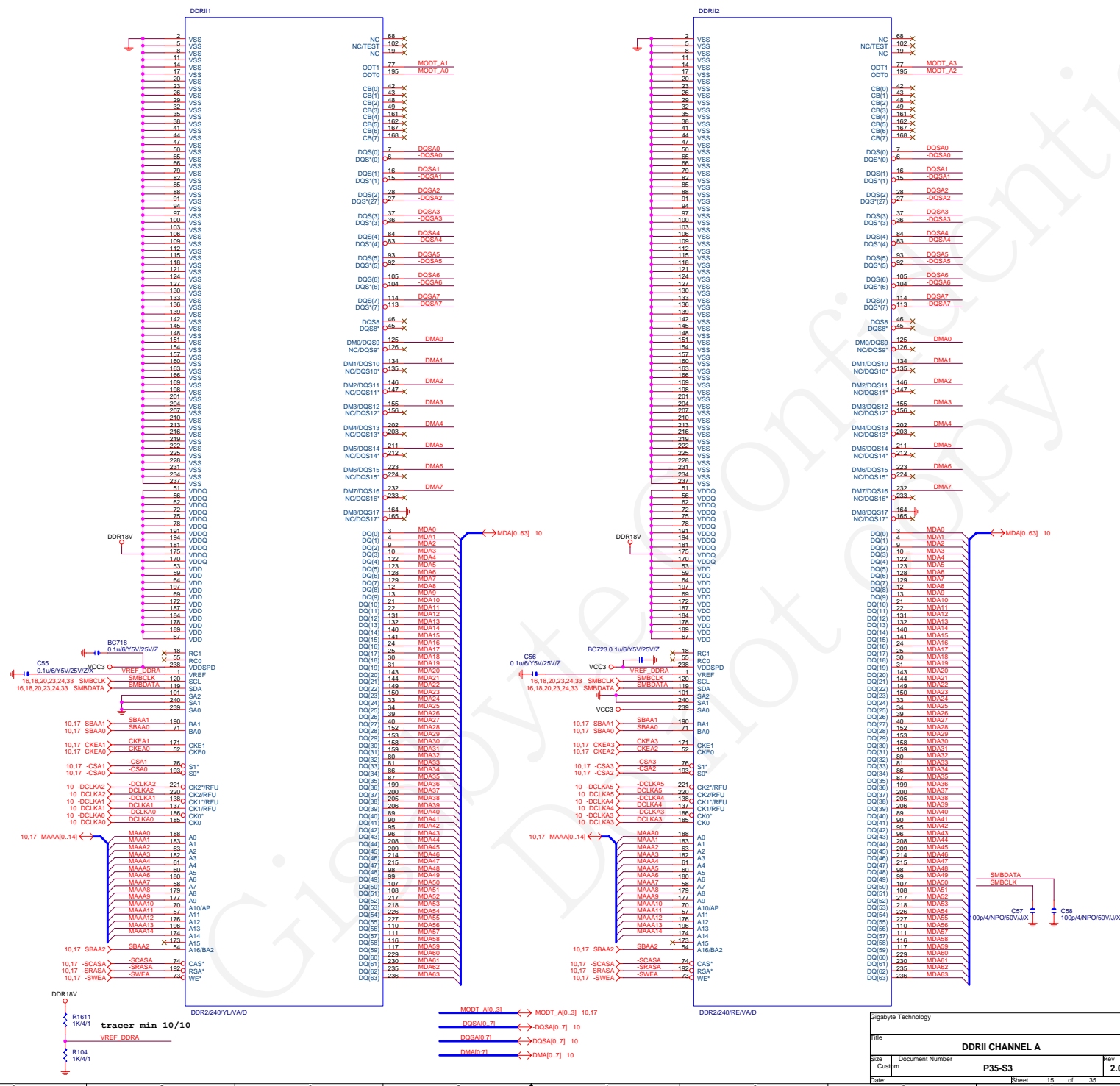
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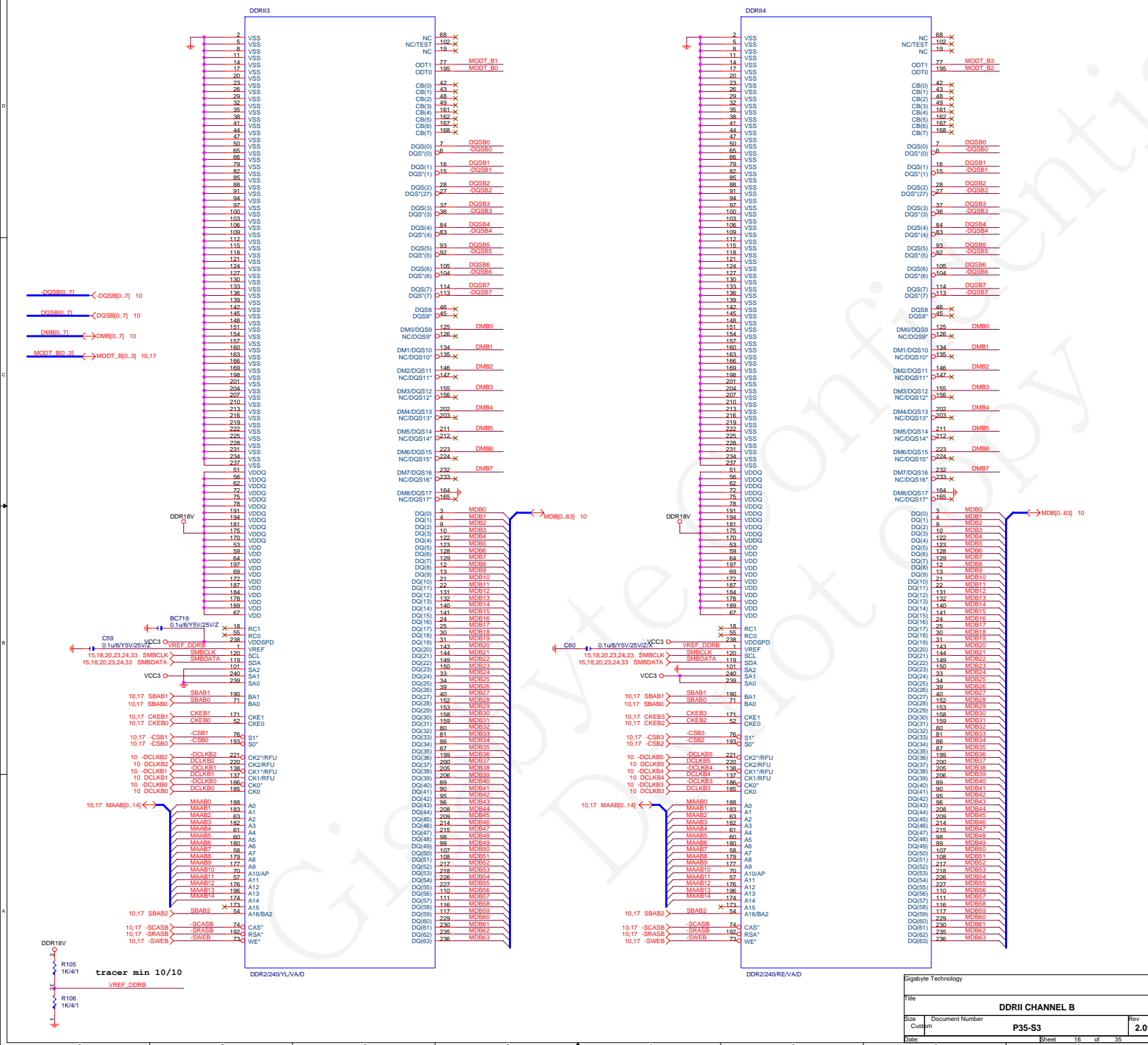
Gigabyte Technology

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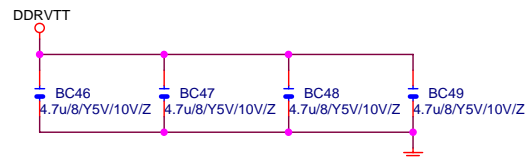
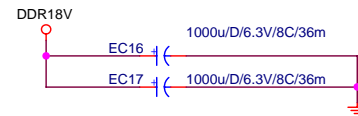
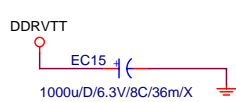






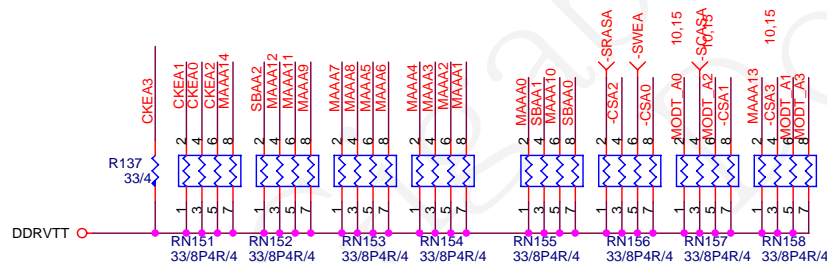
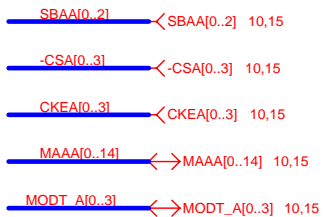
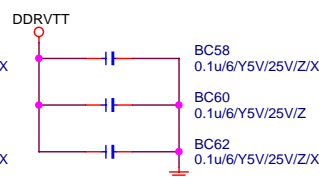
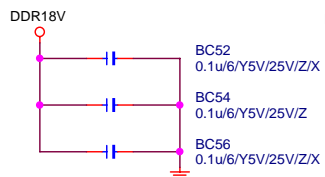
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### DDR18V Decouple

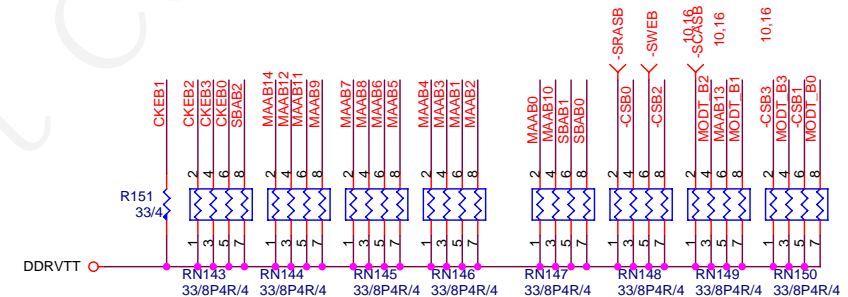
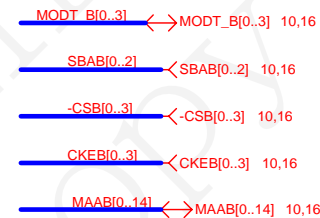
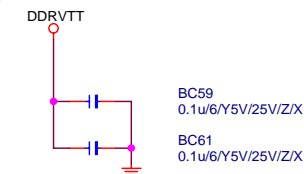
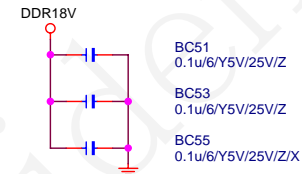
### DDRVTT Decouple



## DDR TERMINATION CHANNEL B

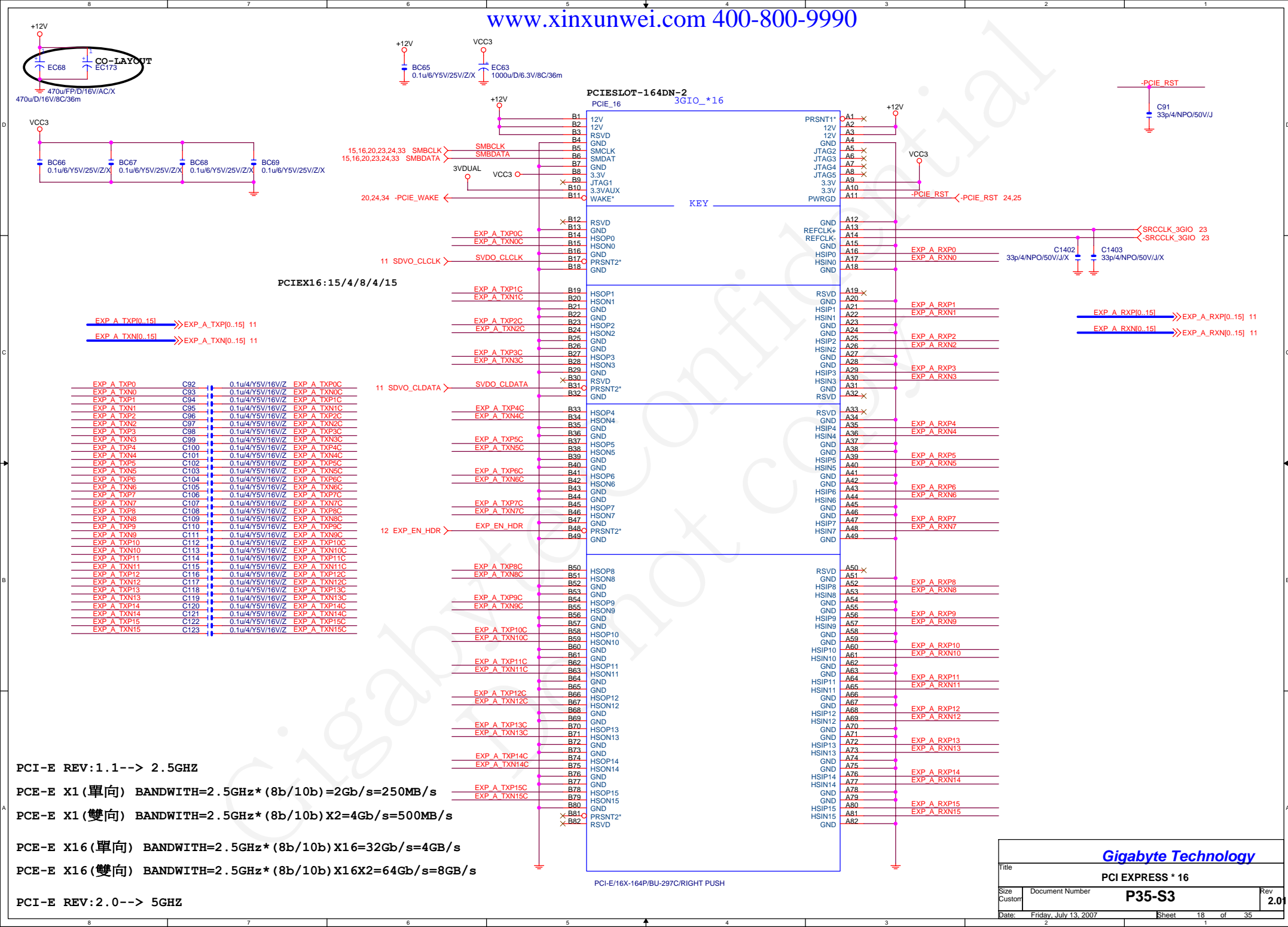
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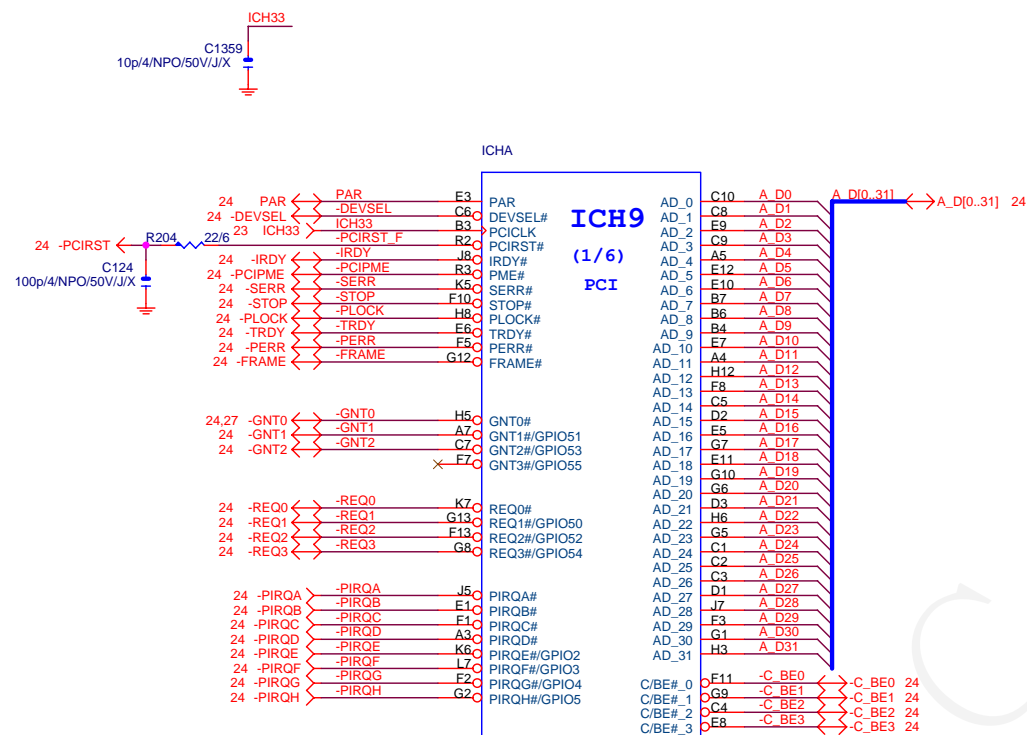
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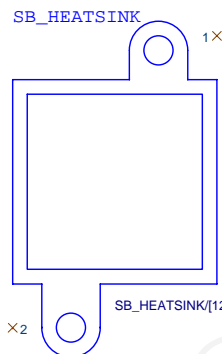
**Gigabyte Technology**

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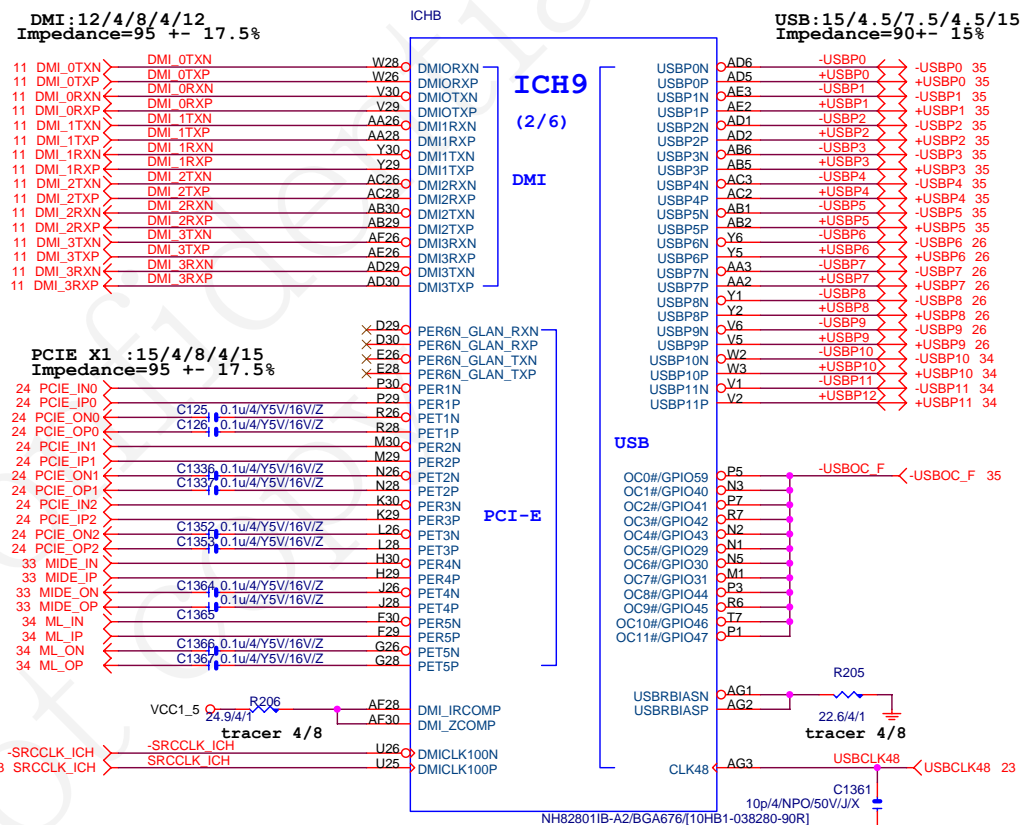




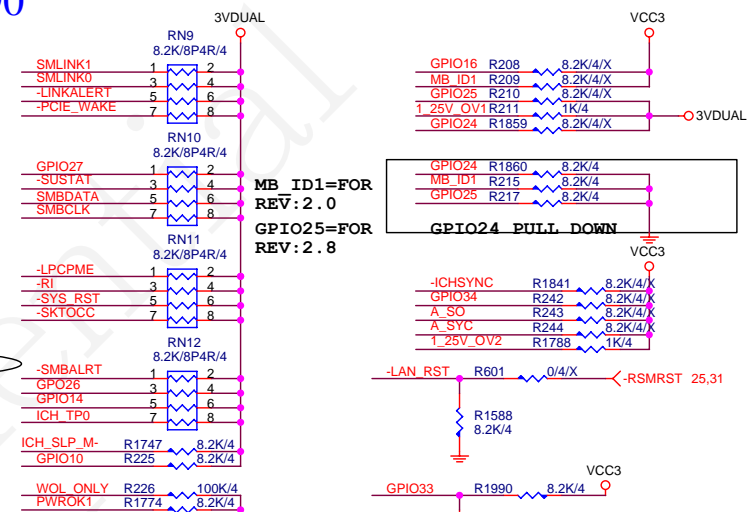
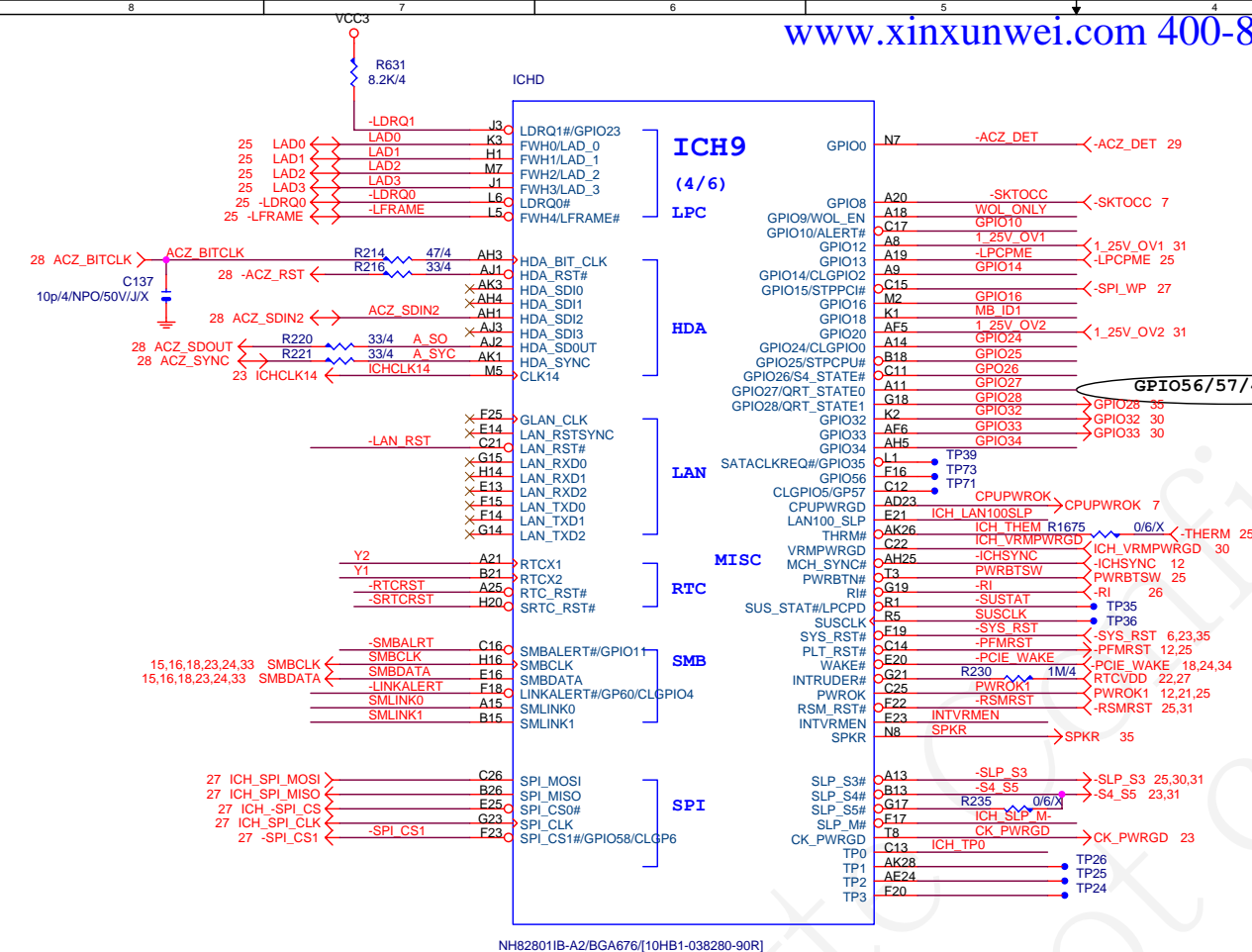
NH82801IB-A2/BGA676/[10HB1-038280-90R]



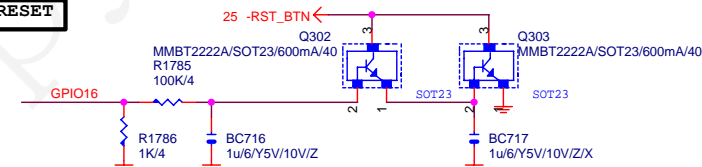
SB HEATSINK/[12SP2-030010-B1R 12SP2-030010-B2R 12SP2-030010-B3R 12SP2-030010-B4R]



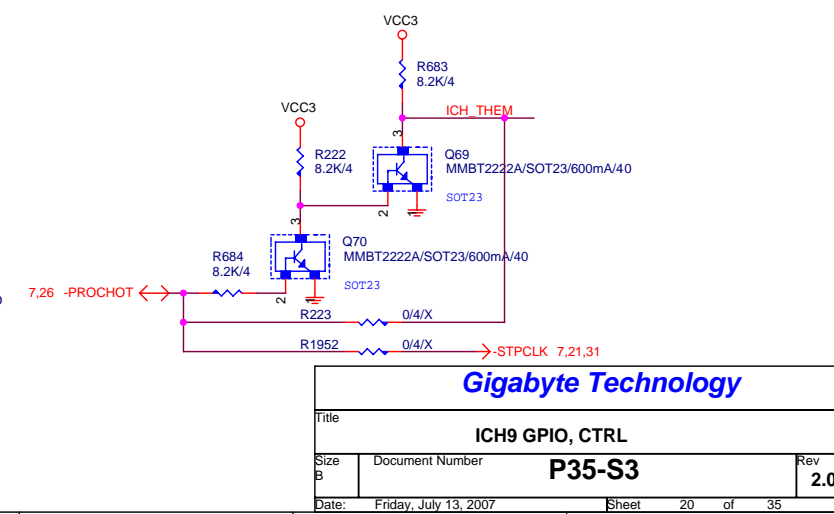
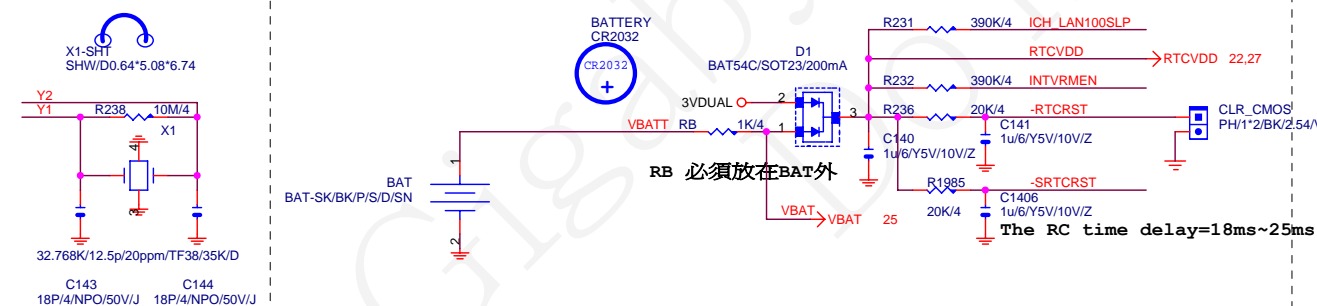
<b><i>Gigabyte Technology</i></b>			
Title			
<b>ICH9-PCI, DMI, LAN, USB</b>			
Size B	Document Number		Rev
	<b>P35-S3</b>		<b>2.0</b>
Date:	Friday, July 13, 2007	Sheet	19 of 35

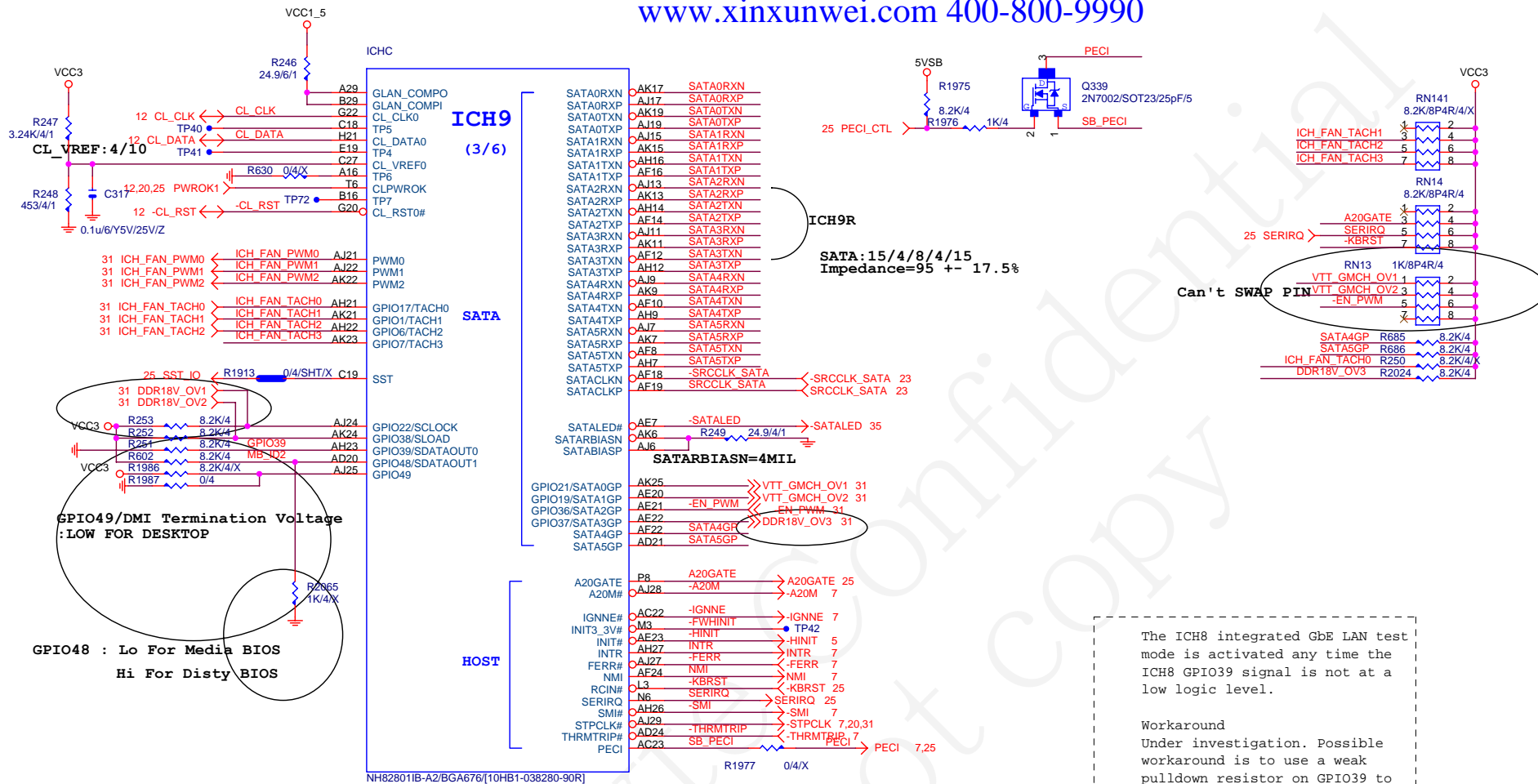


## H/W RESET



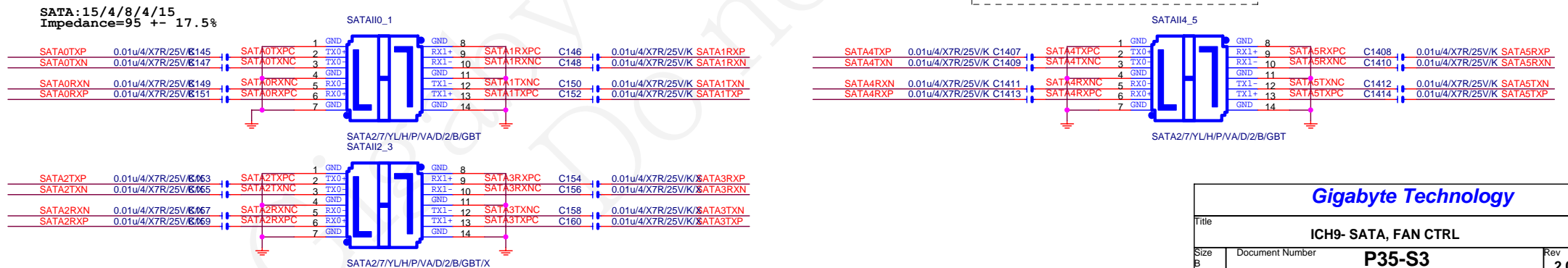
FOR ICH7R POWER ON 瞬間會HIGH 到1.8V 之後0V,必須PULL DOWN 1K/6



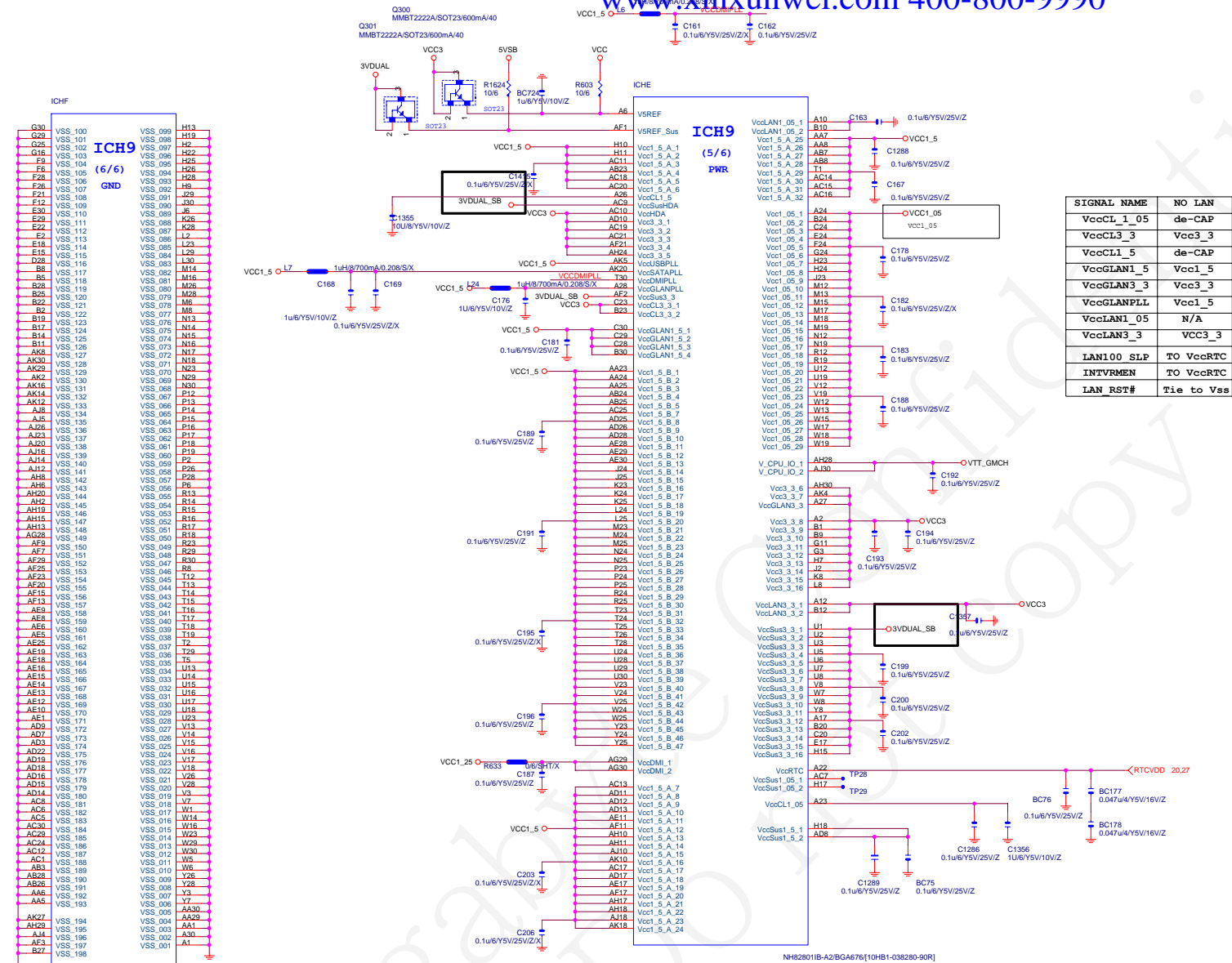


The ICH8 integrated GbE LAN test mode is activated any time the ICH8 GPIO39 signal is not at a low logic level.

Workaround  
Under investigation. Possible  
workaround is to use a weak  
pulldown resistor on GPIO39 to  
ensure signal is always low







SIGNAL NAME	NO LAN
VccCL_1_05	de-CAP
VccCL3_3	Vcc3_3
VccCL1_5	de-CAP
VccGLAN1_5	Vcc1_5
VccGLAN3_3	Vcc3_3
VccGLANPLL	Vcc1_5
VccLAN1_05	N/A
VccLAN3_3	VCC3_3
LAN100 SLP	TO VccRTC
INTVRMEN	TO VccRTC
LAN RST#	Tie to Vss

CLK GEN CK505

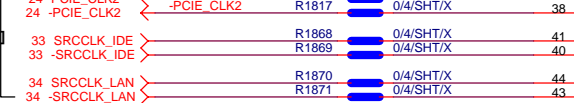
50歐姆: [18/4/10/4/18]



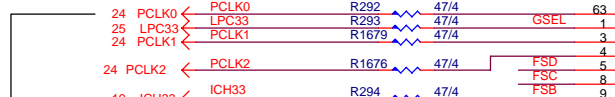
50歐姆: [18/4/10/4/18]



50歐姆: [18/4/10/4/18]



50歐姆: [4/10]



50歐姆: [4/10]

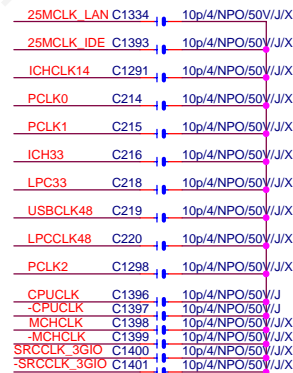
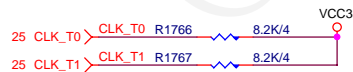
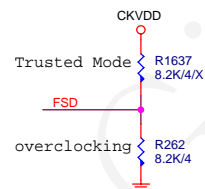
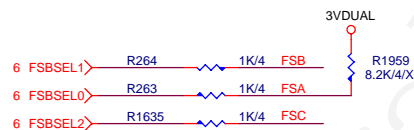
50歐姆: [4/10]



GSEL=1,96Mhz from 14/15,SATACLK from 17/18  
GSEL=0,SATACLK from 14/15,PCIECLK from 17/18

RESET\_IN#/RESET#  
Vtt\_PwrGd/PD#/WOL\_STOP#  
\*\*RLATCH

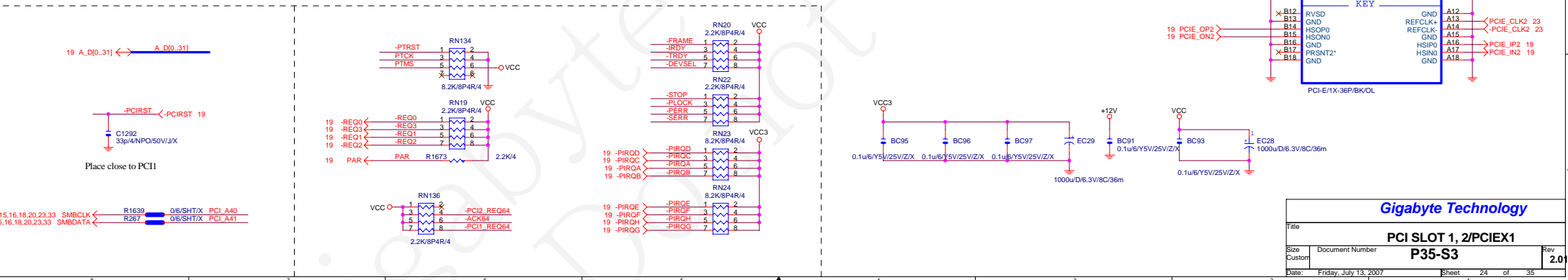
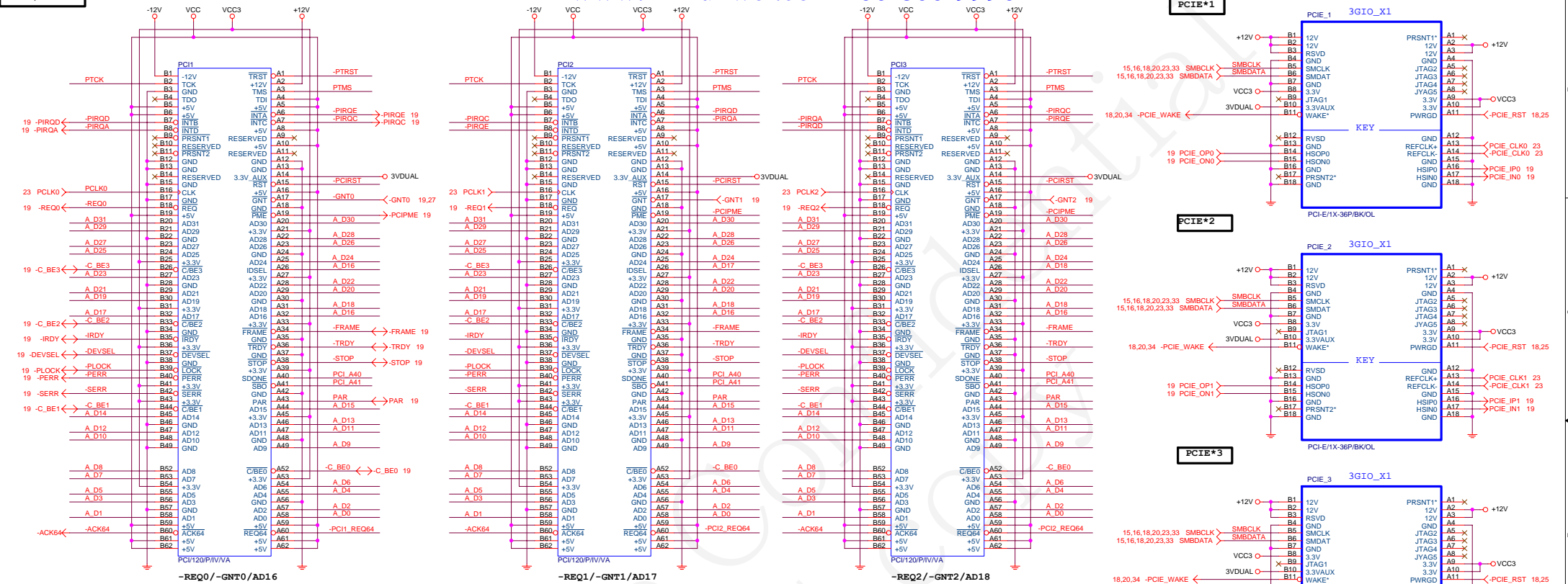
ICS9LPRS87EGLF-T/TSSOP64



Gigabyte Technology

Title			
CK505 CLK GEN			
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PCI1,2 SLOT



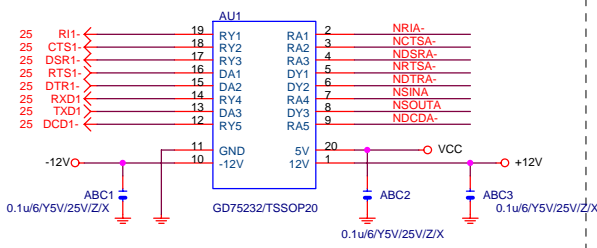
Gigabyte Technology

Title		
PCI SLOT 1, 2/PCIEX1		
Size	Document Number	Rev
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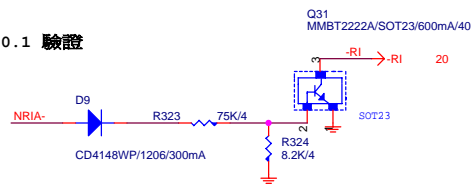


COMA

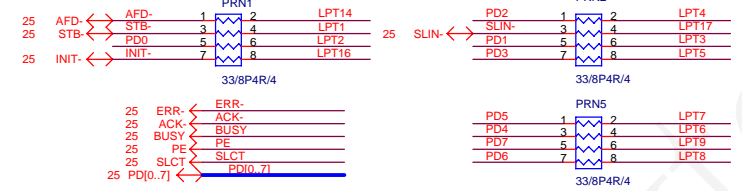


COM R1

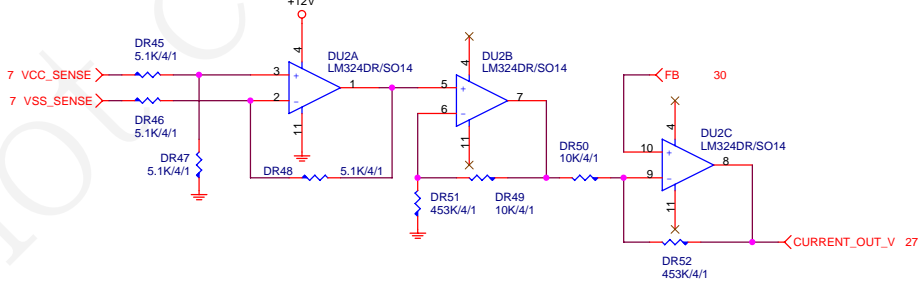
REV:0.1 驗證



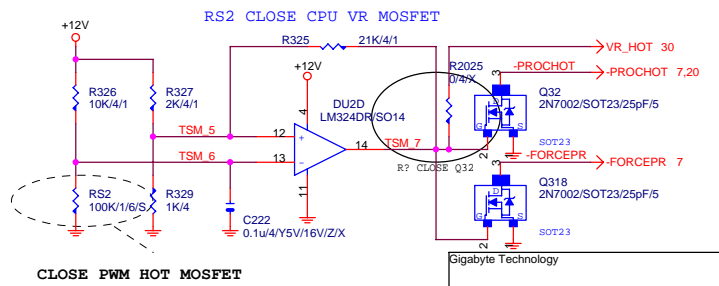
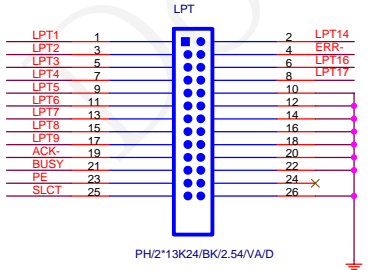
LPT PORT



DYNAMIC CURRENT OC



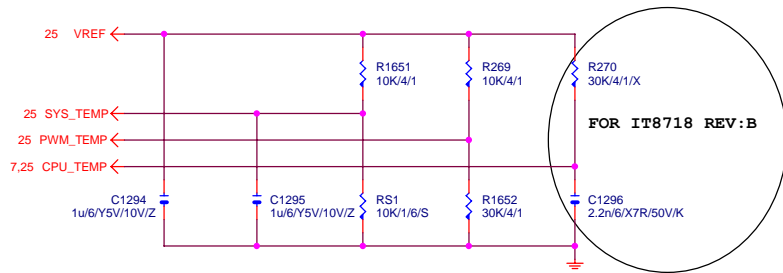
-PROHOT



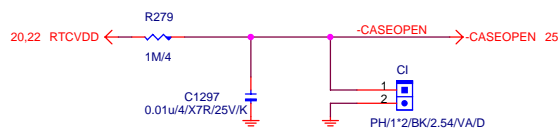
asserted at 131 degree  
deasserted at 116 degree

Gigabyte Technology			
Title			
COM & LPT PORT			
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TEMP H/W MONITOR

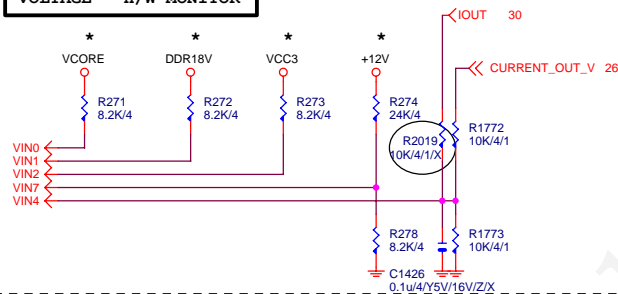


## CASE OPEN

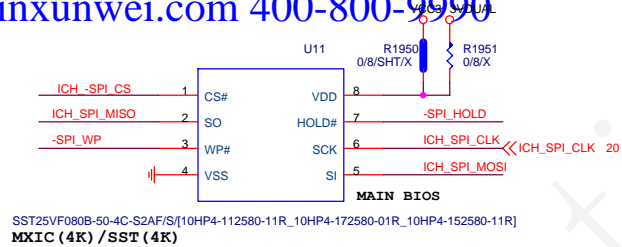
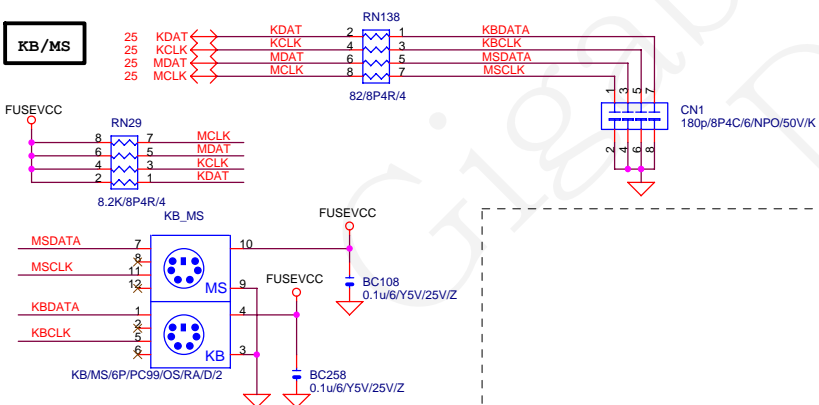


## Case Open Circuits

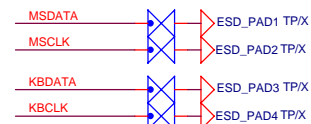
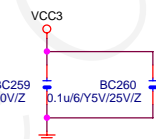
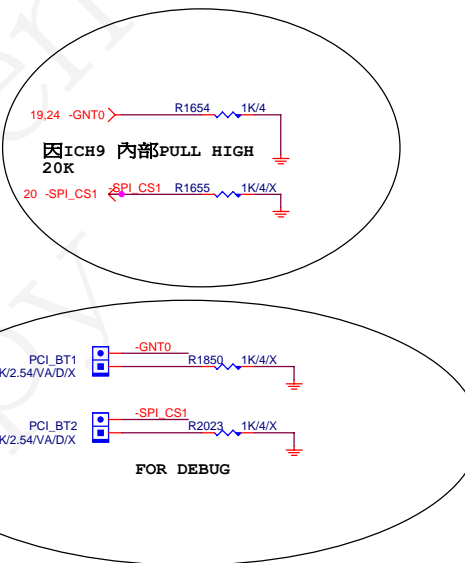
VOLTAGE-- H/W MONITOR



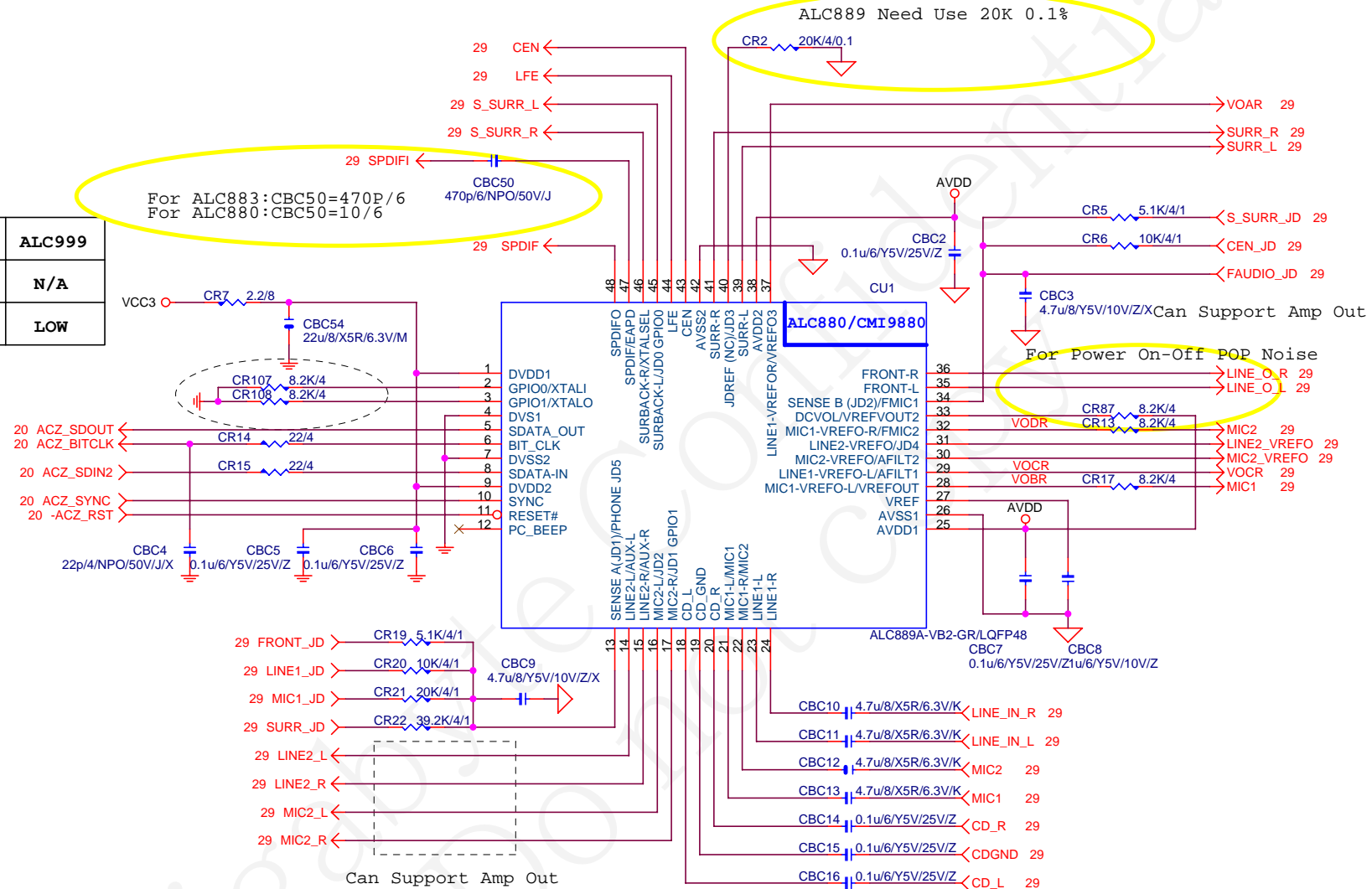
## KB/MS



BOOT DEVICE	GNT0	CS1
SPI	0	1
PCI	1	0
FWH	1	1



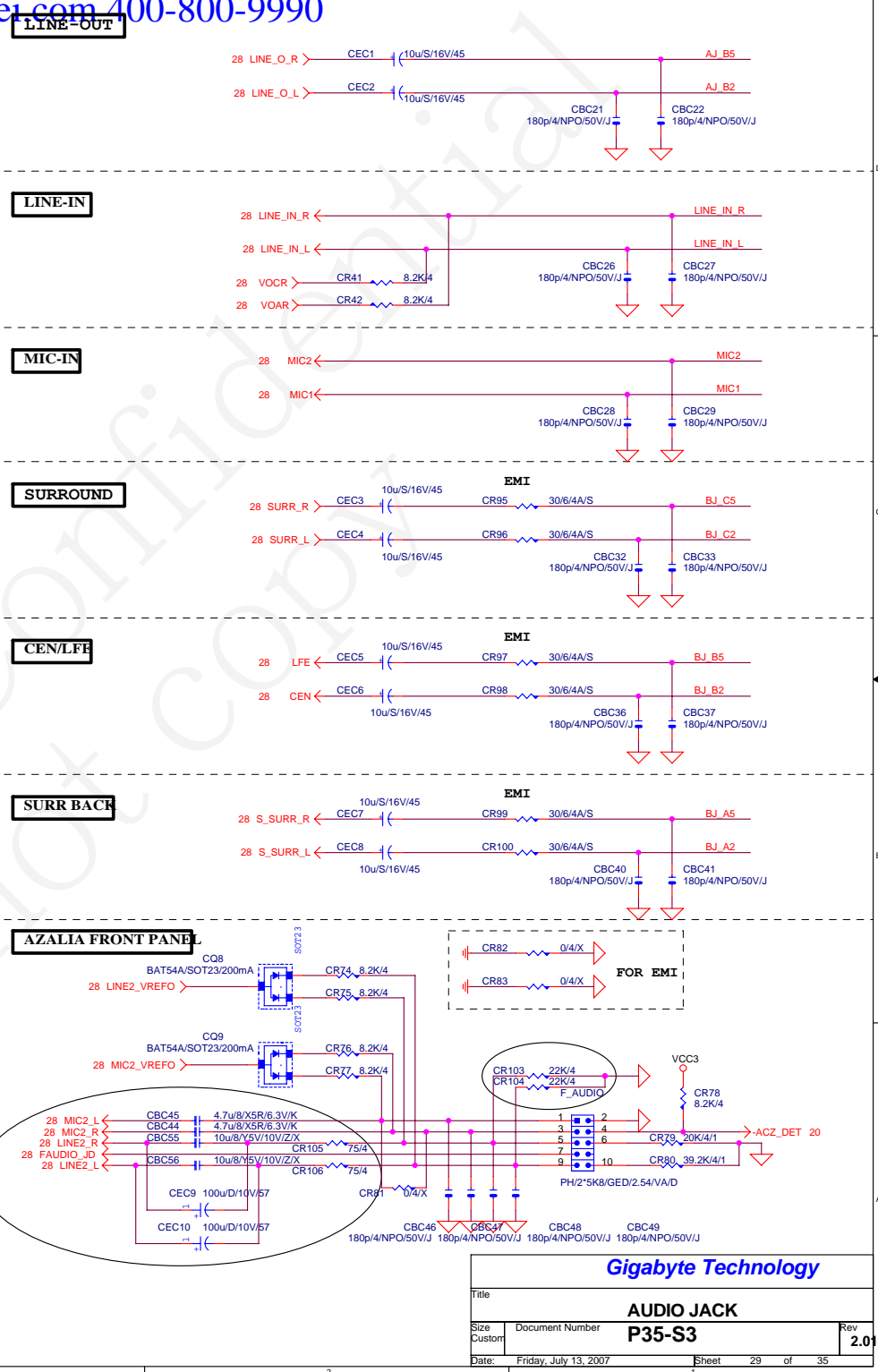
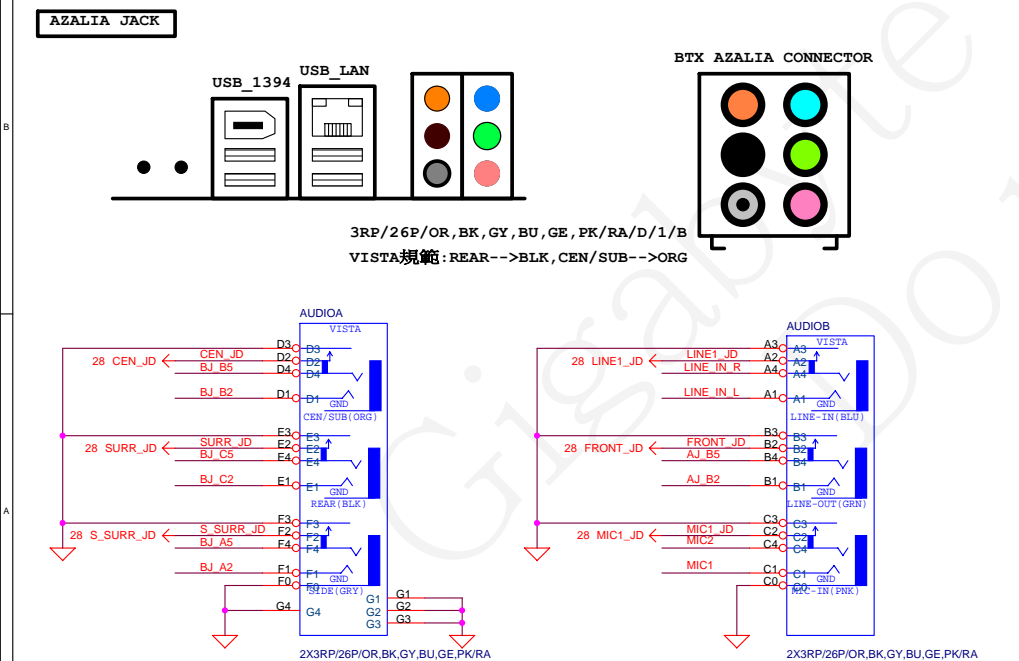
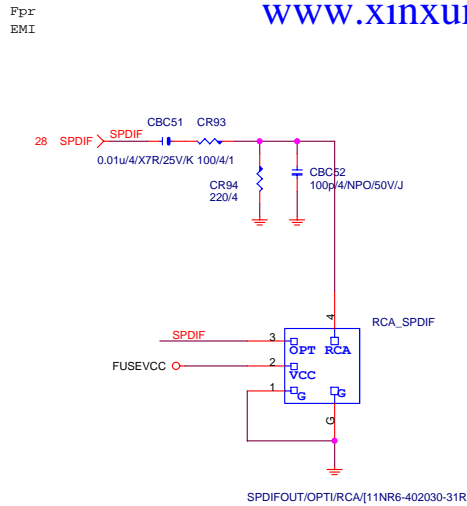
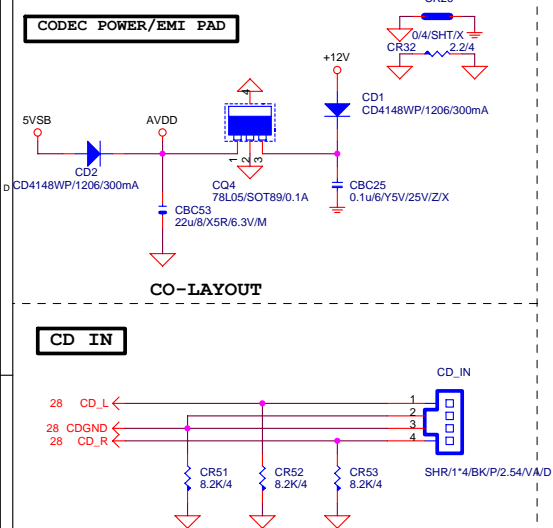
	ALC889A	ALC999
GPIO0	LOW	N/A
GPIO1	LOW	LOW

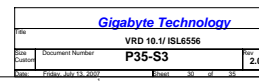


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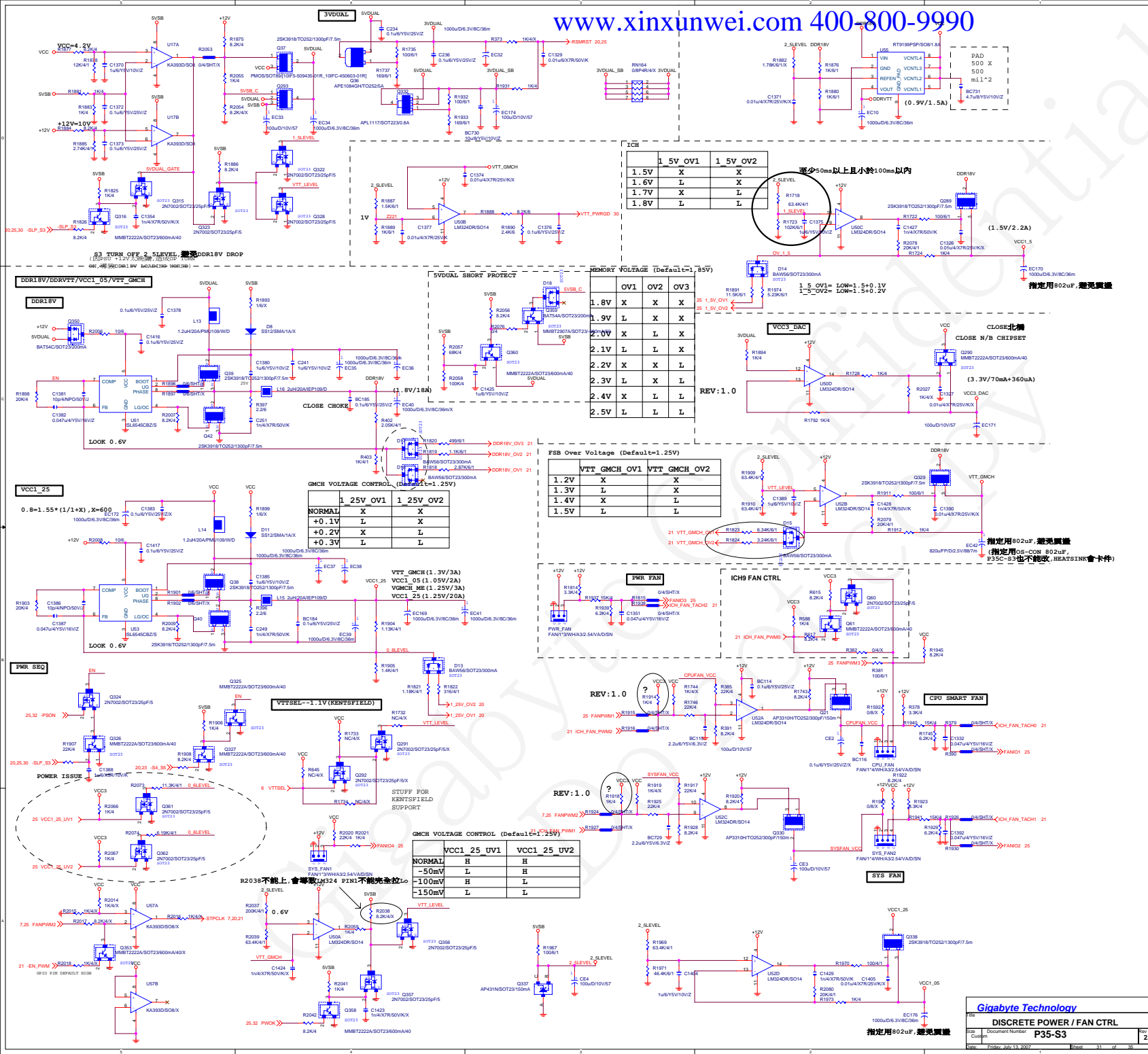
20 ACZ_SDOUT <
20 ACZ_SYNC <
20 -ACZ_RST <
20 ACZ_BITCLK <
20 ACZ_SDIN2 <

```

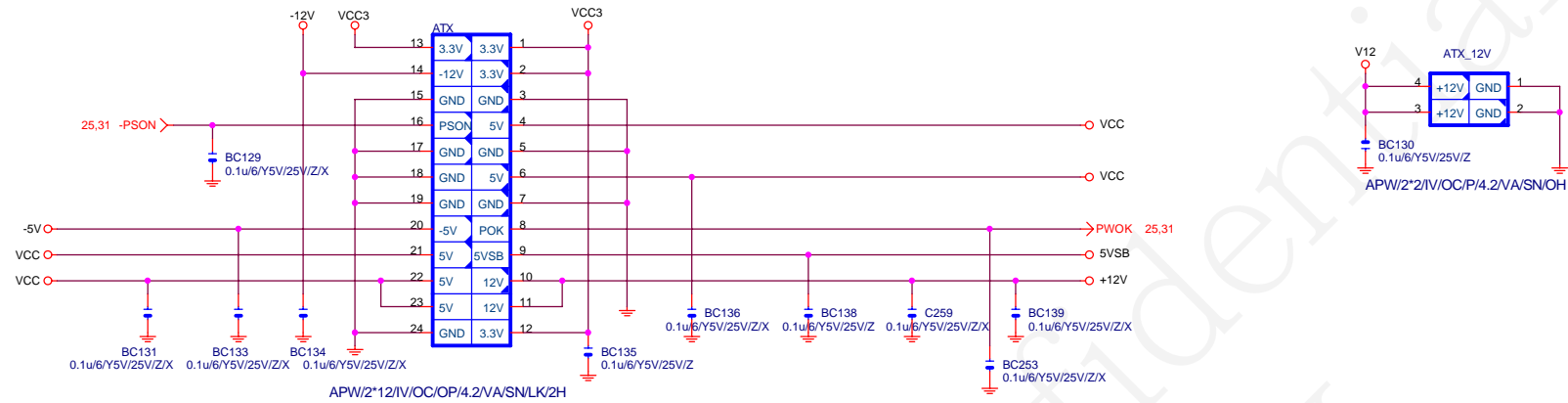




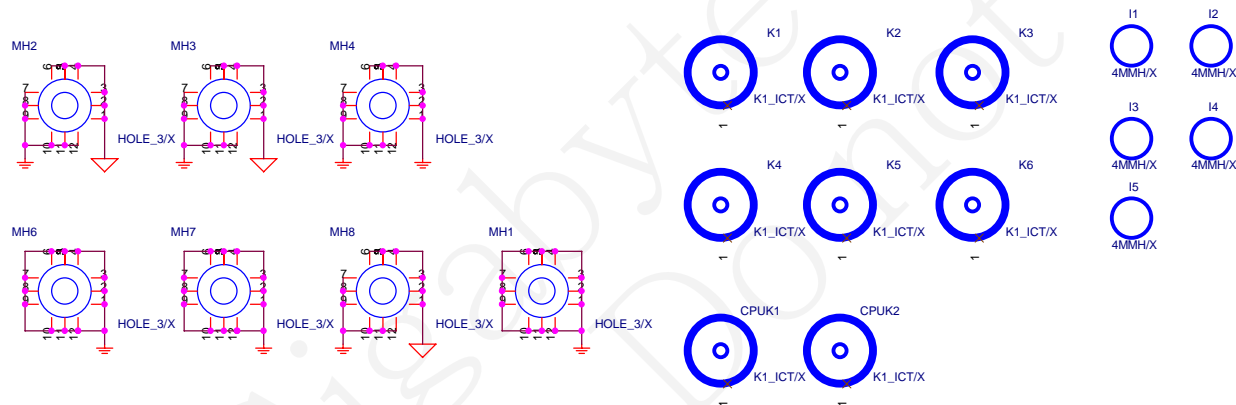




## ATX POWER CONNECTOR



HOLE\_3-2---&gt;有鉛

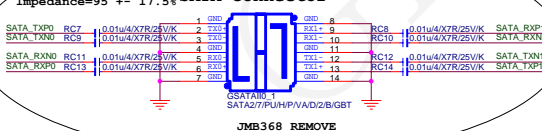
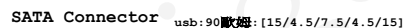
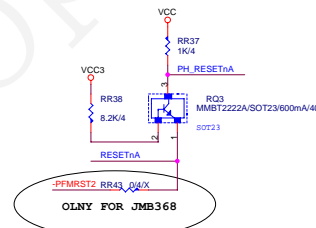
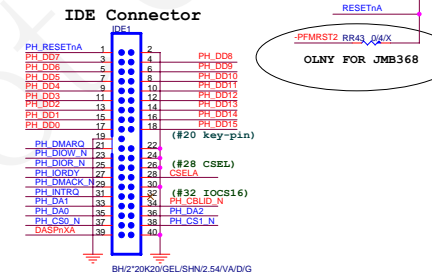
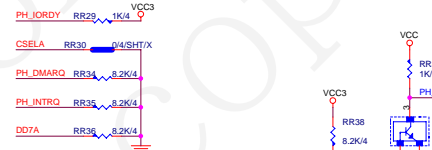
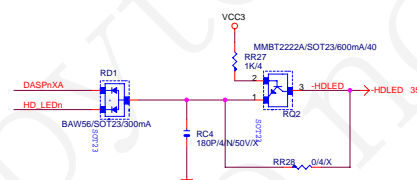
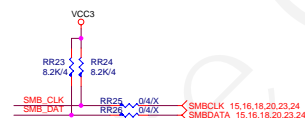
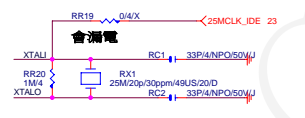
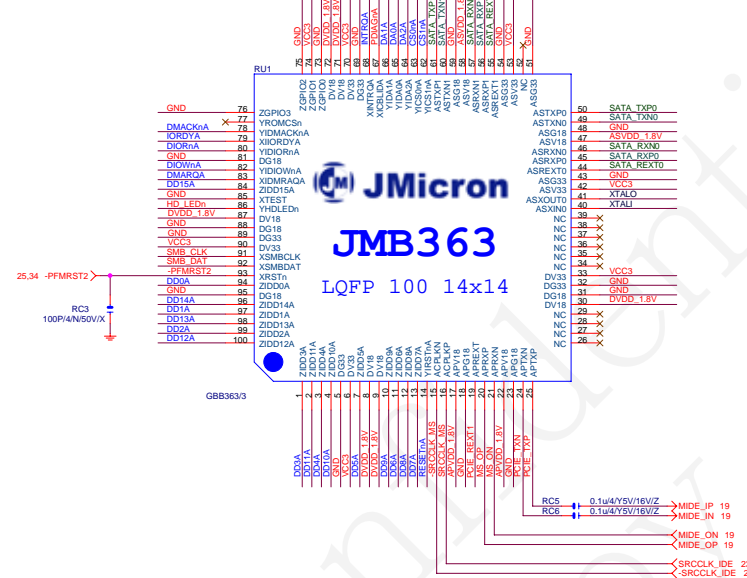
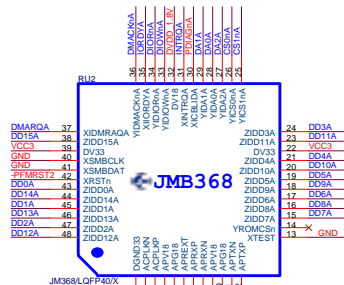
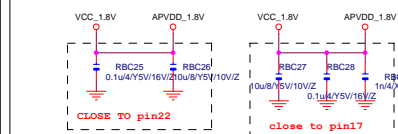
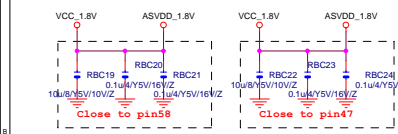
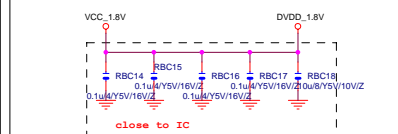
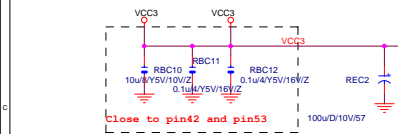
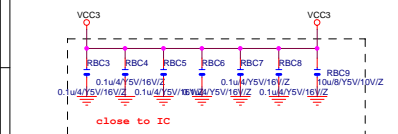
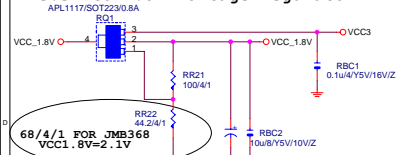


Gigabyte Technology

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ATX POWER CONNECTOR			
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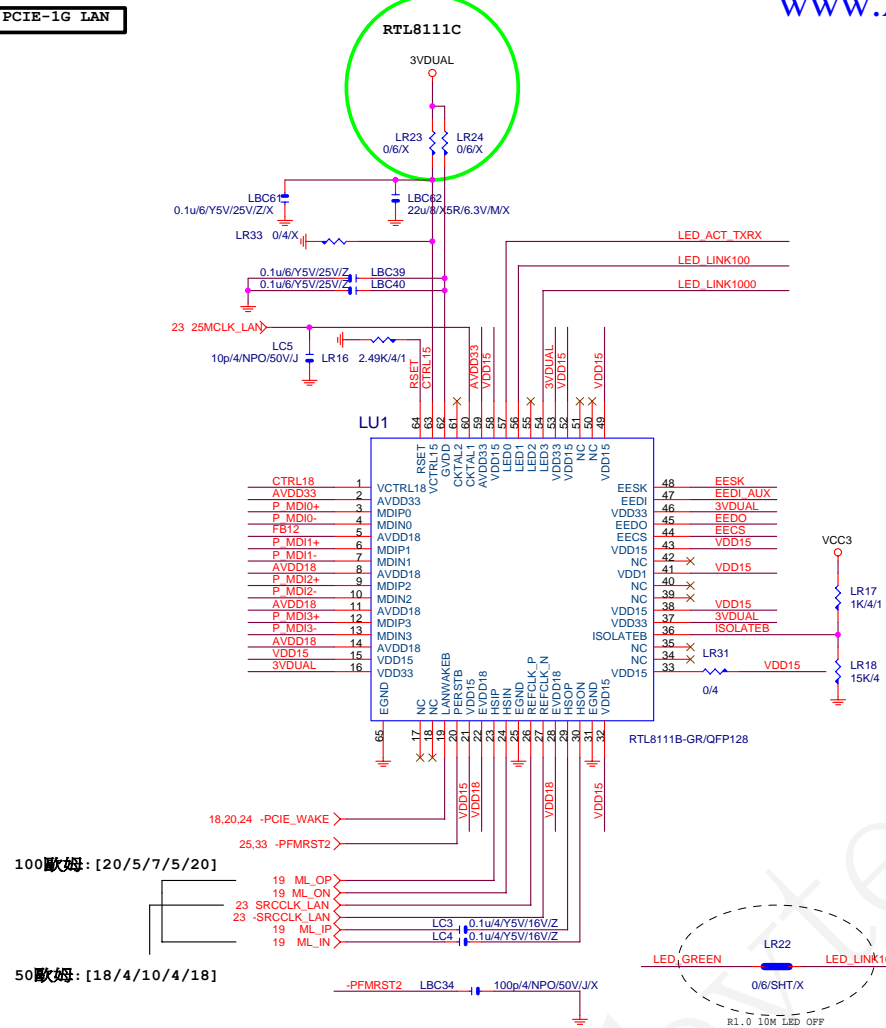


### 3.3V to 1.8V Voltage Regulator



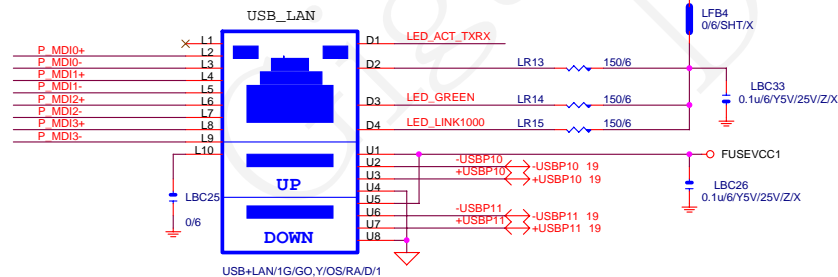
JMB368 REMOVE

## PCIE-1G LAN

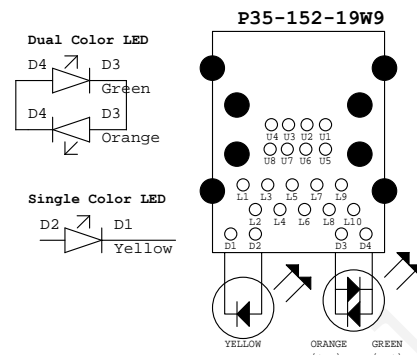


## USB LAN CONNECTOR

LAN 100歐姆:[30/4/8/4/30] FOR B 製程

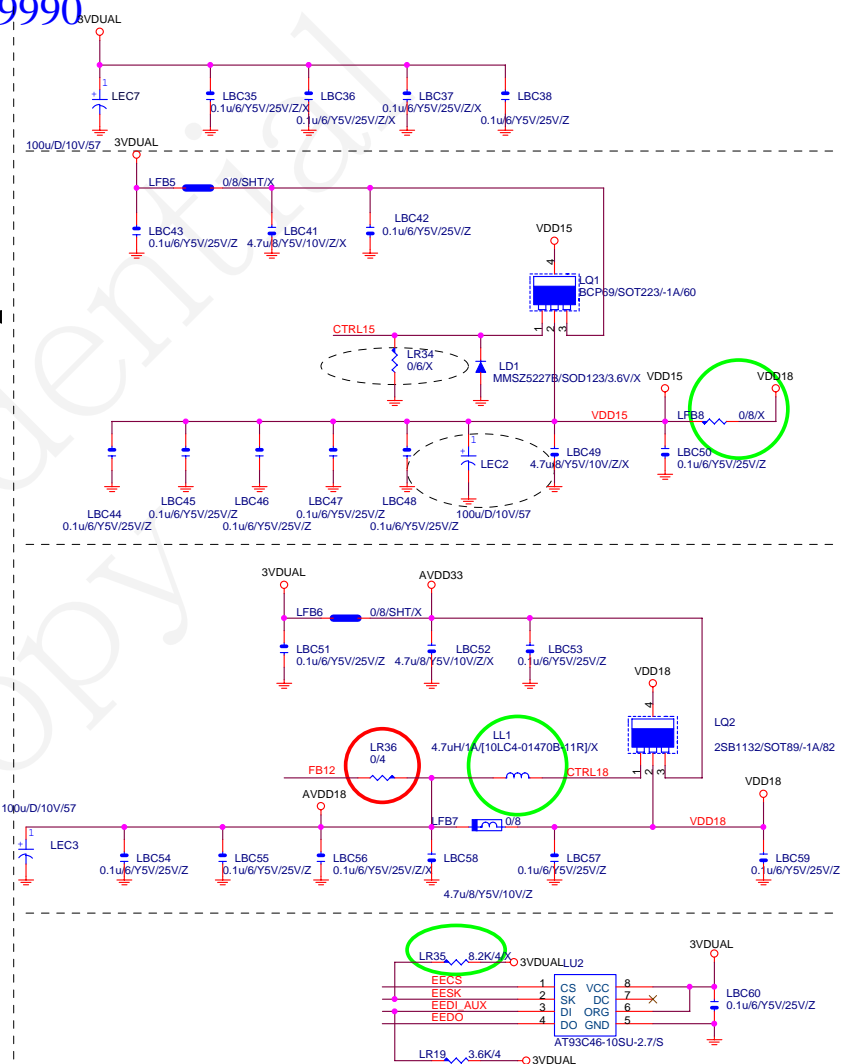


90歐姆: [15/4.5/7.5/4.5/15]

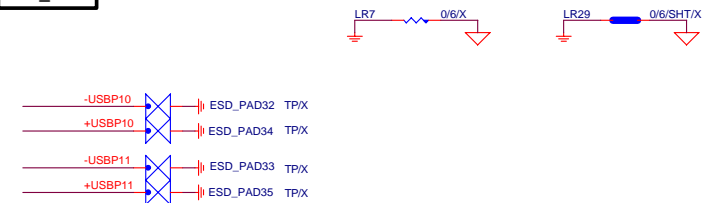


### Power domain chart

	RTL8111B / RTL8101E	RTL8111C	
AVDD33	3.3V	3.3V	
AVDD18	1.8V	1.2V	
EVDD18	1.8V	1.2V	
DVDD15	1.5V	1.2V	



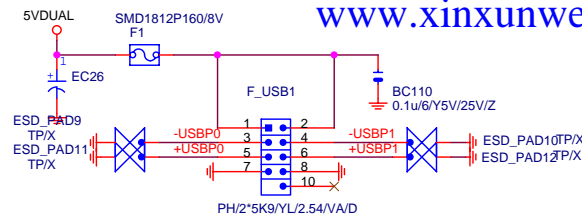
USB\_LAN



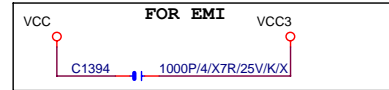
## FRONT USB1

19 +USBP0 <-> +USBP0  
19 -USBP0 <-> -USBP0  
19 +USBP1 <-> +USBP1  
19 -USBP1 <-> -USBP1

1000u/D/6.3V/8C/36m

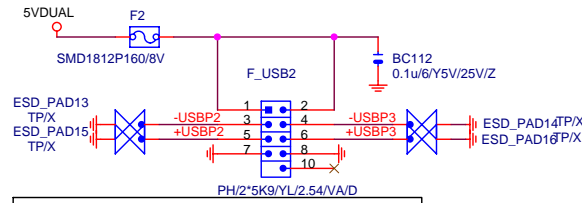


FOR EMI

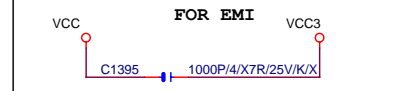


## FRONT USB2

19 +USBP2 <-> +USBP2  
19 -USBP2 <-> -USBP2  
19 +USBP3 <-> +USBP3  
19 -USBP3 <-> -USBP3



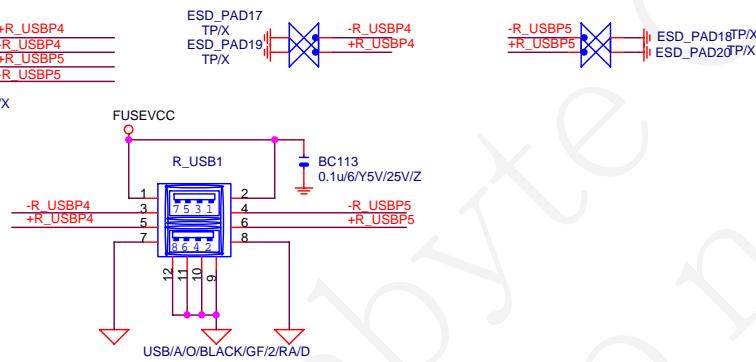
FOR EMI



## R\_USB1

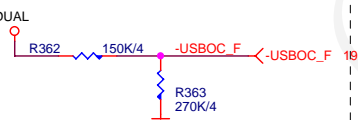
19 +USBP4 <-> +USBP4  
19 -USBP4 <-> -USBP4  
19 +USBP5 <-> +USBP5  
19 -USBP5 <-> -USBP5

SRN2  
0/8P4R/SHT/X

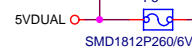


## FRONT USB OC1

## USB POWER



320MILS



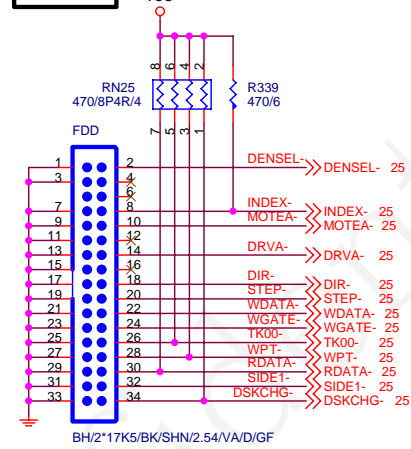
160MILS

FUSEVCC

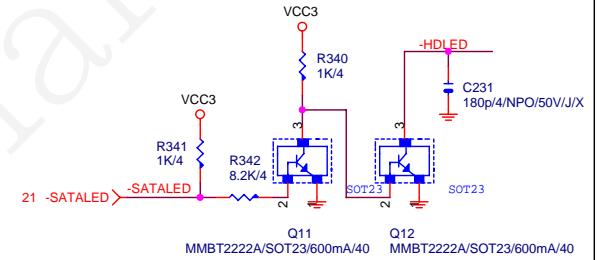
FUSEVCC1

BC105

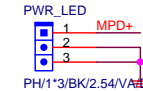
## FLOPPY



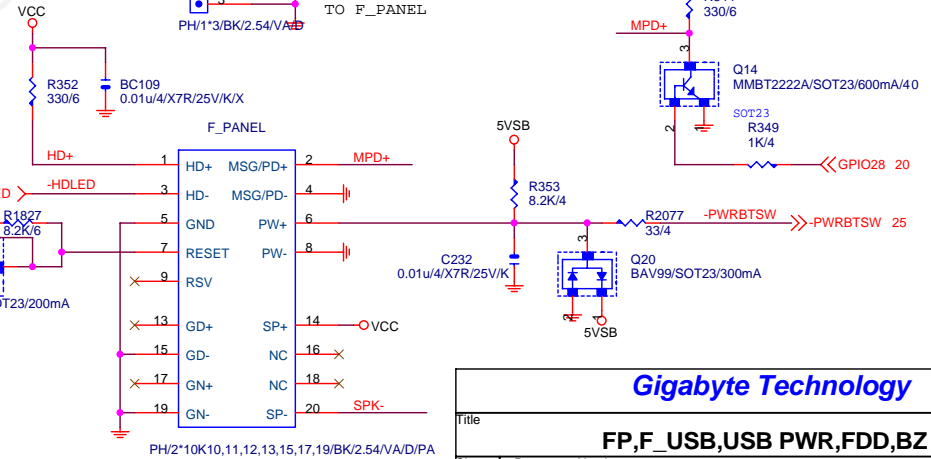
## SATA LED



## INTEL FRONT PANEL



3 PIN POWER LED  
LAYOUT PLACE CLOSE  
TO F\_PANEL



Gigabyte Technology

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